The CAD Library

by Tom Hausherr

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http://www.pcbdesign007.com/pages/columns.cgi?clmcatid=&clmid=58

Introduction

This is a series intended to help the reader create a high-quality CAD library. The CAD library is the starting point that affects every process from engineering and PCB layout through PCB manufacturing and assembly.

Guidelines and Recommendations

When creating a CAD library, there are dozens of things to consider that are often overlooked or not even considered that will directly affect the quality of part placement, via fanout, trace routing, post processing, fabrication, and assembly processes. This article, Part 1 of a series, introduces aspects that should be considered when creating CAD library parts and the impact that each feature of the CAD library has on the PCB process. Subsequent articles will delve more deeply into these concepts.

A high-quality CAD library can make a huge difference in the quality of your PCB design layout and your overall productivity levels throughout the PCB design process. Also, you must have the necessary tools that can quickly build new CAD library parts – parts that are consistent in quality, with identical features in every library part. You also need an organized CAD library management system that allows you to quickly locate the correct land pattern for each component in your PCB layout.

To begin, all of the components and their related land patterns can be found in the free LP Viewer that you can download by clicking here.

Creating a CAD Library

Creating a CAD library requires answers to these questions:

Why do we snap the lands (pads) to a 0.1 mm grid?

Why is the assembly outline different than the silkscreen outline?

Why do we snap the via fanout to a 1 mm grid?

Why is it important to use metric units when creating your CAD library?

What is the IPC-7351B standard and why is it important?

Every good PCB designer has the heart of an artist and the mind of a mathematician, and each PCB design is a different piece of art with mechanical precision. Good PCB designers take pride in their workmanship as they strive to make each new PCB layout more perfect than the last. After 35 years of laying out over 2,000 PCB designs, I can say without any reservation that PCB design perfection starts in the CAD library.

Measurement Units

One of the secrets of today is that 90% of all component manufacturers are providing their component package dimensions and pin pitches in metric units. Texas Instruments only provides metric units for all 982 of their component packages. TI is following the metric mandate set by all world standards organizations and 99% of all world governments. So your CAD library should also be built using metric

units.

Using metric units for PCB design layout is the future, so you should transition to metric as soon as possible and quit wasting your time building an Imperial unit working environment. The longer you wait to transition, the harder it becomes. If you're a PCB design artist in search of perfection, this series of columns will clearly illustrate why metric units for PCB layout is vastly superior.

The IPC-7351B Standard

Let's briefly look at the IPC-7351B Standard. We will reference this standard throughout the series. IPC-7351B standard uses a 3-Tier CAD library system:

Most land protrusion (Density Level A) – for military and medical applications

Nominal land protrusion (Density Level B) – for controlled environment desktop

Least land protrusion (Density Level C) – for cell phones and hand held devices

The IPC-7351B standard focuses on these key items:

Land size and spacing calculations

Placement courtyard boundary

Land pattern name

Zero component orientation

Padstack name

Three types of CAD library parts are defined: Plated through-hole (PTH), surface mount devices (SMD), and a combination of the two technologies. SMD and PTH CAD libraries are distinctively different but the same basic rules apply to both technologies – "snap" and "round-off" CAD library land (pad) shapes are defined in 0.05 mm increments.

We will look at why this standard is so important and how it relates to our CAD library shortly in the series.

In addition to the items in the IPC-7351B standard, other important considerations are basic guidelines and drafting recommendations for your CAD library. These are summarized here and will be fully explored as we continue.

Pad spacing with DRC checking and pad trimming when necessary

Pad size and space round-off

Four outlines

Silkscreen

Assembly

Placement courtyard – adjustable sizing for IPC 3-Tier environment levels

3D model

Polarity Markings for both silkscreen and assembly

Two reference designators with center/center justification (Ref Des Origin), right reading orthogonal, located at the land pattern origin with height 1.5 mm and line width 10% of Height

The 1608 (EIA 0603) Chip Component

Chip components make up the majority of the parts on a normal PCB layout. These chip components have a “wraparound” lead form. My last PCB layout had 698 capacitors, 386 chip resistors, and 81 chip inductors. The entire design had 1,250 parts and 1,165, or 93%, were chip components. So, it is very important that we address chip components first in this series.

The majority of chip components are metric by design, i.e., 90% of all chip component dimensions are whole metric values. See Figure 1 for the dimensions of a standard 1608 (EIA 0603) component superimposed with its related land pattern (in blue) and placement courtyard excess of 0.25 mm. Notice that the placement courtyard is 3.0 mm X 1.5 mm. That dimension is perfect for placing this land pattern using a 0.5 mm grid system — they all line up perfectly.

The land size and centric placement are rounded in 0.05 mm increments to enhance trace routing using a 0.05 mm routing snap grid and trace widths in 0.25 mm increments.

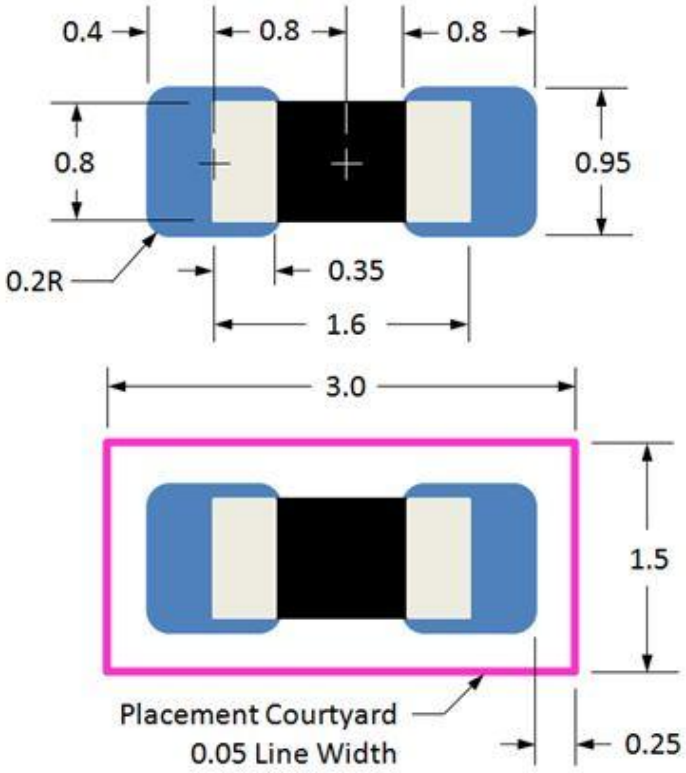


Figure 1. Standard 1608 (EIA 0603) component superimposed with its related land pattern (in blue) and placement courtyard excess of 0.25 mm.

Figure 2 illustrates four of the most popular trace/space routing technologies that use a 0.05 mm routing grid. The six most popular metric trace widths rounded in 0.25 mm increments are:

1. 0.075 mm (3 mils)
2. 0.1 mm (4 mils)
3. 0.125 mm (5 mils)
4. 0.15 mm (6 mils)

5. 0.2 mm (8 mils)
6. 0.25 mm (10 mils)

The main point that I am trying to make here is that with most CAD tools, using a PCB design grid system is best. One exception to this is the Mentor Graphics Expedition Enterprise, which handles gridless solutions. But for users of other industry tools, building CAD libraries, part placement, via fanout and trace routing using specific snap grids greatly enhances the speed and quality of the PCB layout.

The standard universal grid system today is 0.05 mm, but at times 0.025 mm increments need to be used specifically for trace/space rules.

The next generation of grid systems in the near future will be 0.01 mm, which I refer to as “high resolution.” There will likely never be a need to go more than 2 places to the right of the decimal point for any PCB design feature values.

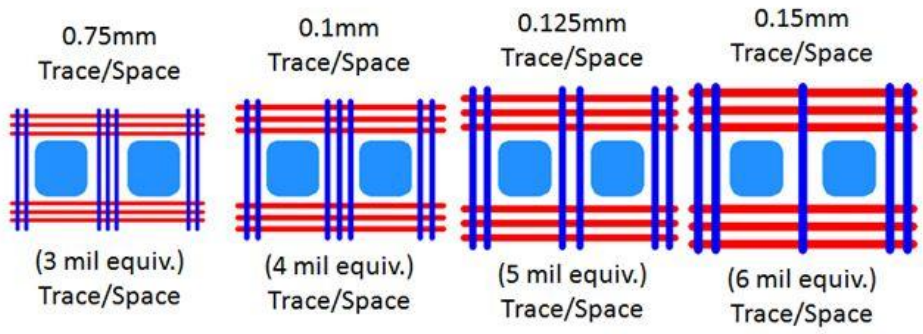


Figure 2. Comparison of four popular trace/space routing technologies that use a 0.05 mm routing grid.

The same chip component technology can be applied to every chip resistor and capacitor used in the industry today. The most relevant aspect of this technology is that a 0.1 mm placement grid and a 0.05 mm routing grid system produce optimized results regardless of the trace/space technology, because the land (pad) center snap grid is 0.05 mm from the origin and the land (pad) size round-off values are in 0.05mm increments.

Fanout

Let’s talk about via fanout solutions for the same 1608 (EIA 0603) chip capacitor. In Figure 3 you can see two different fanout options, and one is superior to the other. The fanout coming out the top has all the key features. The vias are 0.4 mm closer to the capacitor component terminals than the typical right/left fanout, which decreases impedance and increases capacitance.

Also, the top fanout vias snap to a 1 mm grid because the 1608 land pattern was snapped to a 0.5 mm grid system. The 0.5 mm via land (pad) diameter with 0.25 mm hole size and 0.7 mm plane anti-pad is perfect for 0.1mm trace/space technology. See Figure 4 for the routing solutions. The trace width for the power fanout is 0.3 mm.

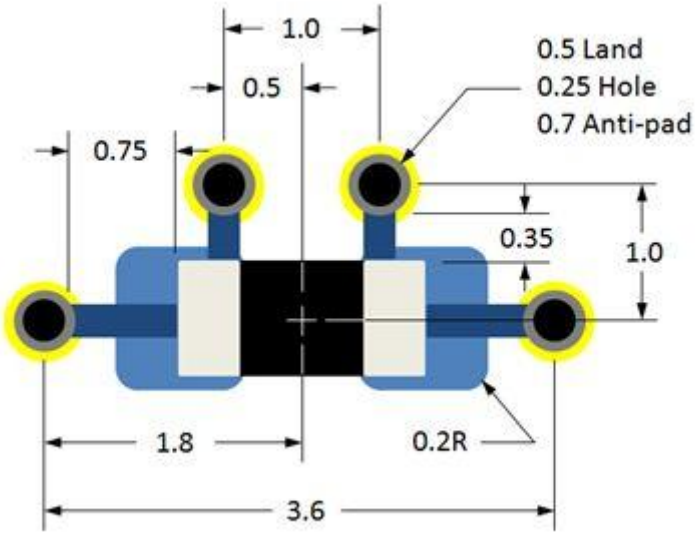


Figure 3. Two different fanout options.

Figure 3 clearly illustrates the superior routing channels between two vias placed on a 1 mm snap grid. This same example can be used for all chip and molded body resistors and capacitors. It is important to note that the plane anti-pad clearance does not infringe on the trace. The trace requires a clean uninterrupted return path on the adjacent reference plane. This via land, hole size, and trace/space technology is very easy to manufacturer and does not require additional fabrication cost.

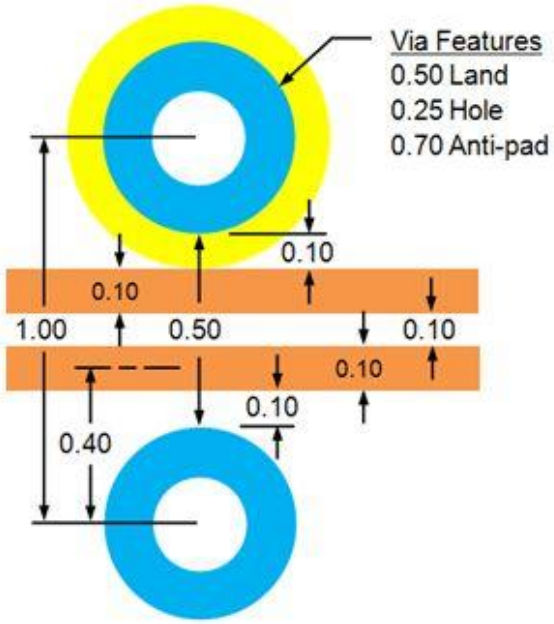


Figure 4. Graphic depicting routing solutions.

The part placement of the 1608 (EIA 0603) can use a 0.5 mm snap grid and the placement courtyards can be placed side by side. The via fanout can be a 1 mm snap grid when exiting the side of the land pattern; otherwise, when exiting the top and bottom, a 0.1 mm snap grid can be used. See Figure 5 for

the placement and fanout example for the 1608 (EIA 0603) chip components. Side via fanout is superior for bypass capacitors connecting to the planes and best for 1 mm via snap grid. The top and bottom fanout is OK for signal resistors.

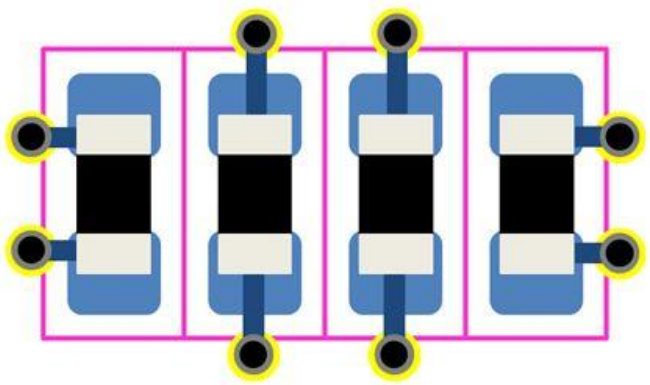


Figure 5. Placement and fanout example for the 1608 (EIA 0603) chip components.

Components Smaller Than 1608 (EIA 0603)

When chip component sizes are smaller than 1.6 mm X 0.8 mm, the IPC-7351B standard defines seven rule changes that every PCB designer and CAD librarian must be aware of:

The land (pad) snap grid changes from 0.1 mm to 0.02 mm

The land size round-off changes from 0.05 mm to 0.01 mm

The toe goal changes from 0.35 mm to 0.2 mm

The corner radius changes from 0.2 mm to 0.15 mm

The courtyard excess changes from 0.25 mm to 0.15 mm.

When entering the component min/max dimensions the “nominal” terminal dimensions are used for both the min & max fields

The part placement grid changes from 0.5 mm to 0.1 mm

1005 (EIA 0402) Design

See Figure 1 for the dimensions of a standard 1005 (EIA 0402) component superimposed with its related land pattern. In this case, I decided to break the rules:

Land size round-off 0.05 mm

Land snap grid round-off 1.0 mm

Tighten the tolerance on the component width (W = 0.5 mm) to +/-0.05

The land-center to land-center spacing is 1.0 mm, which is perfect for 1.0 mm space via fanout. And the placement courtyard width is 1.0 mm, which is perfect for placing parts 1.0 mm from center to center. When placing the 1005 (EIA 0402) in the PCB layout, use a 0.1 mm grid to optimize the part placement and via fanout.

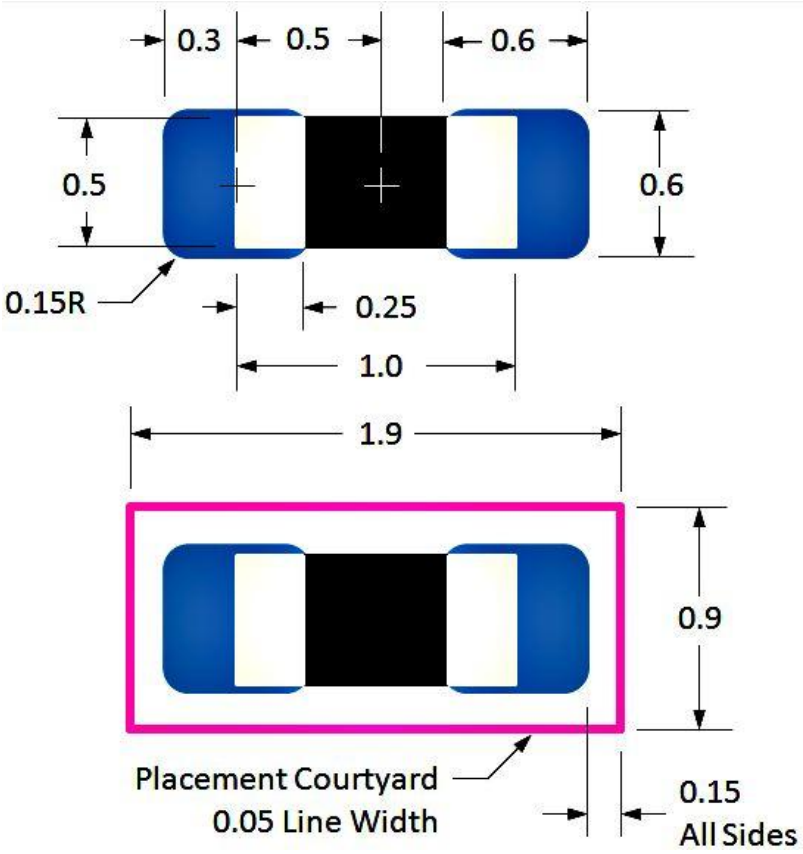


Figure 1. A standard 1005 (EIA 0402) component superimposed with its related land pattern.

The 1005 (EIA 0402) was made for 1 mm pitch BGA fanout. In Figure 2 you can see two different fanout options; one is superior to the other. The fanout coming out the top has all the key features. The vias are 0.25 mm closer to the capacitor component terminals than the typical right/left fanout, which decreases impedance and increases capacitance. Also, the top fanout vias snap to a 1 mm grid because the 1005 land pattern was snapped to a 0.1 mm grid system. The 0.5 mm via land (pad) diameter with 0.25 mm hole size and 0.7 mm plane anti-pad is perfect for 0.1mm trace/space technology. The trace width for the power fanout is 0.3 mm.

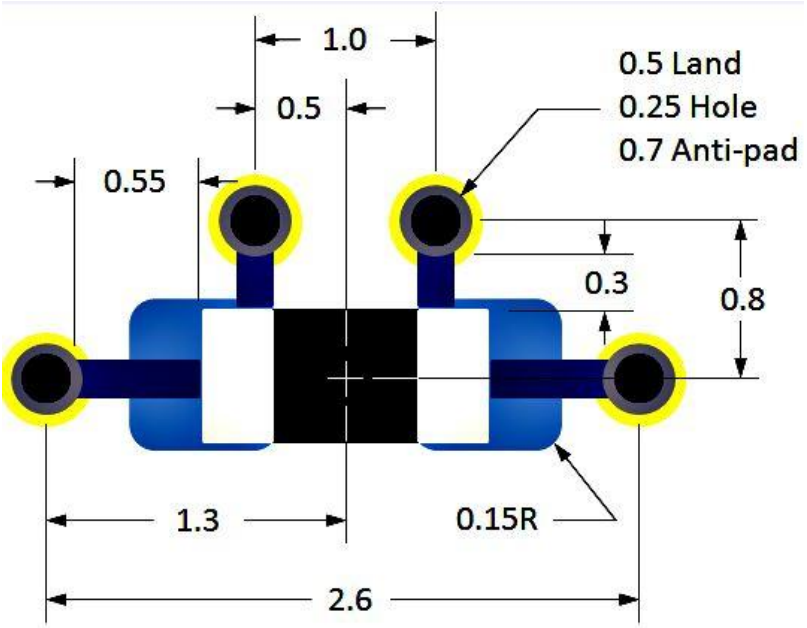


Figure 2. Two different fanout options, one better than the other.

0603 (EIA 0201)

Figure 3 shows the dimensions of a standard 0603 (EIA 0201) component superimposed with its related land pattern. In this case, I decided to break the rules:

Land size round-off 0.05 mm

Land snap grid round-off 1.0 mm

Use the “Least” environment due to component miniaturization

For chip components smaller than 1.0 mm X 0.5 mm, I use the IPC-7351B “Least Environment” to prevent tombstoning. When two-pin micro-miniature parts have too much solder volume, tombstoning can occur in the reflow oven. The land size for the 0603 (EIA 0201) should be a minimum of two times the terminal lead size. The land maximum value is still being tested by assembly shops, as tombstoning is the Number 1 problem with the 0603 (EIA 0201) chip component.

Note: The placement courtyard width is 0.6 mm to compensate for the component width tolerance of +/-.03 mm.

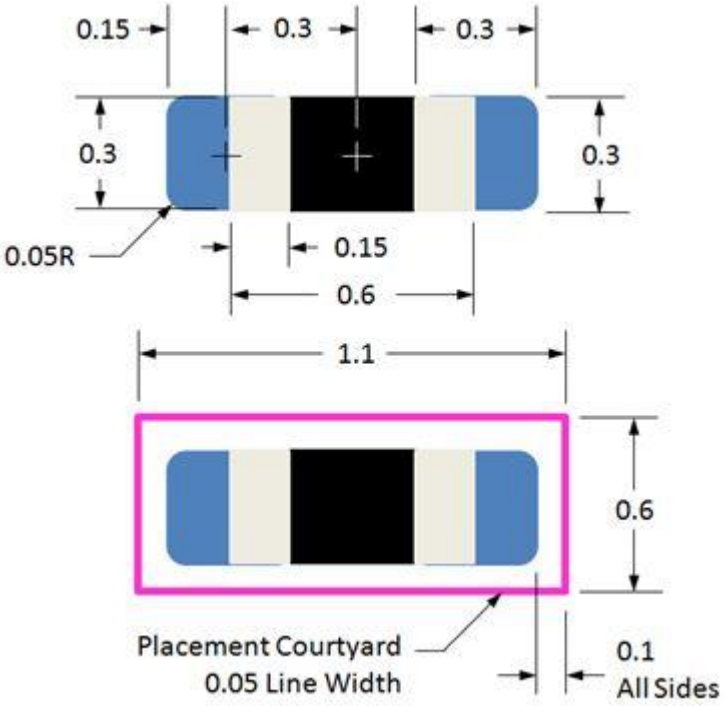


Figure 3. A standard 0603 (EIA 0201) component superimposed with its related land pattern.

One of the techniques used to prevent tombstoning for the 0603 (EIA 0201) is to thin the paste stencil from 0.15 mm to a smaller value for every occurrence of this component in the paste mask stencil, as illustrated in Figure 4. The responsibility of the stencil thickness thinning process is placed on the assembly shop and the stencil manufacturer (not the PCB designer). Assembly shops use various solder alloys that require unique stencil creation.

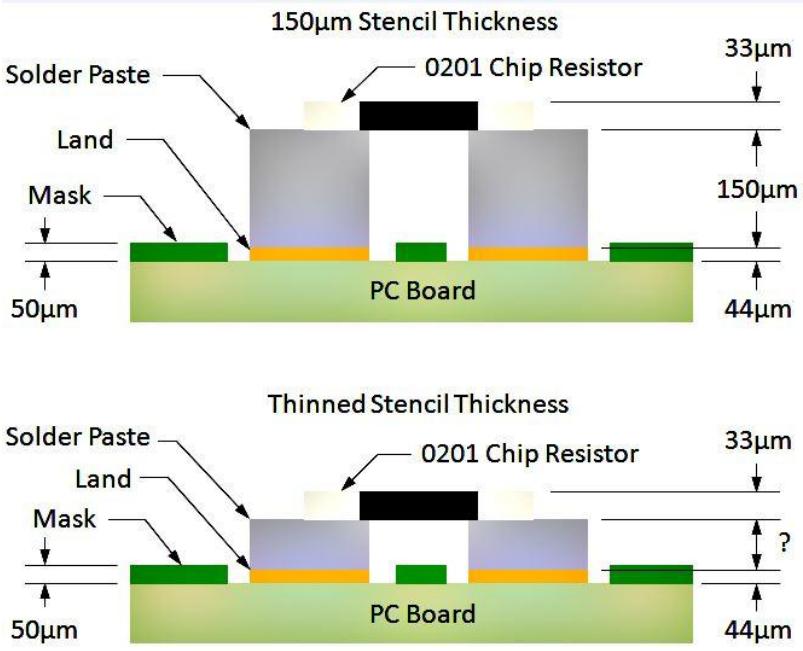


Figure 4. Thinning the paste stencil from 0.15 mm to a smaller value can prevent tombstoning for the 0603 (EIA 0201).

In Figure 5, the dimensions of a standard 0603 (EIA 0201) component are superimposed with its related land pattern. If you normally use the “Most” environment, my recommendation for the 0603 (EIA 0201) land pattern is to use the “Nominal” environment. The IPC nominal land size for the 0603 is about three times the size of the terminal lead. For this 0603 micro-miniature component, stay away from the “Most” environment as the solder volume is more than four times greater than the terminal lead footprint.

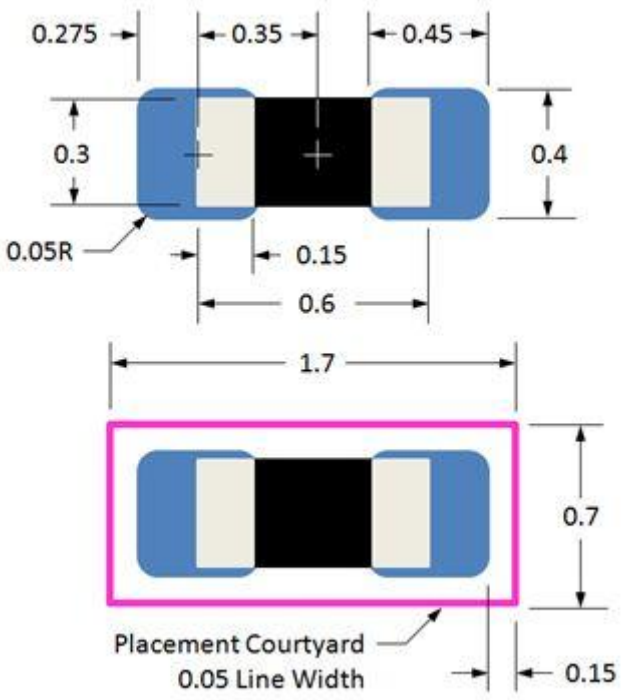


Figure 5. A standard 0603 (EIA 0201) component superimposed with its related land pattern.

The 1005 (EIA 0402) & 0603 (EIA 0201) chip components are very compatible with 1.0 mm pitch BGA. In Figure 6 there are two different uses for the 1005 and one in between the vias and one via-in-pad method. Because the 1005 land centers are on 1.0 mm pitch, the capacitor land (pad) falls directly centered on the via. Via-in-pad technology will increase PCB cost because these vias need to be plated, filled and surface finish on the capacitor pad. The 0603 fall between the vias for the 0.1 mm trace/space technology DRC. This solution will not increase PCB fabrication cost. The dot grid display is 0.05 mm.

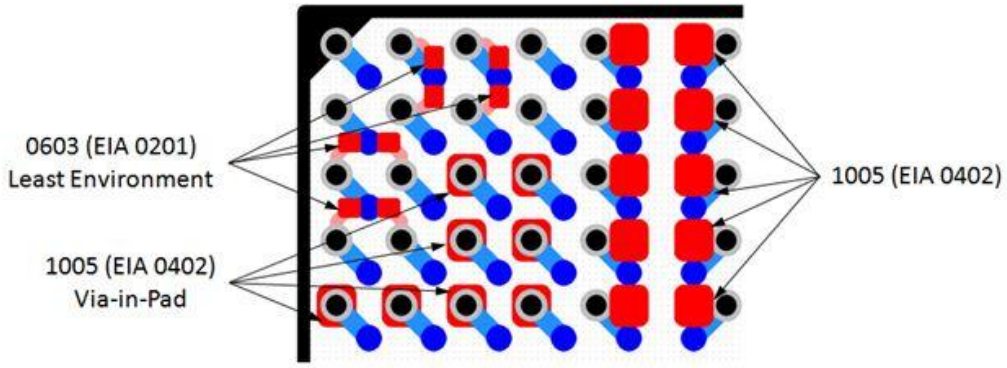


Figure 6. Graphic detailing 1005 (EIA 0402) & 0603 (EIA 0201) chip components.

IPC does not have a “standard” on drafting items such as silkscreen and assembly outlines and polarity markings yet. There are several types of silkscreen outlines and polarity markings that are used for non-polarized chip parts, polarized capacitors, diodes and LED’s.

For a standard non-polarized chip, there are two options. See Figure 7 for both options. One is a line that separates the two lands. The default size is 0.2 mm and the default silkscreen land gap is 0.25 mm. The CAD librarian can change both the line width and the gap to achieve placing a line between two lands that only have a 0.3 mm gap by simply changing the line width and gap rules to 0.1 mm.

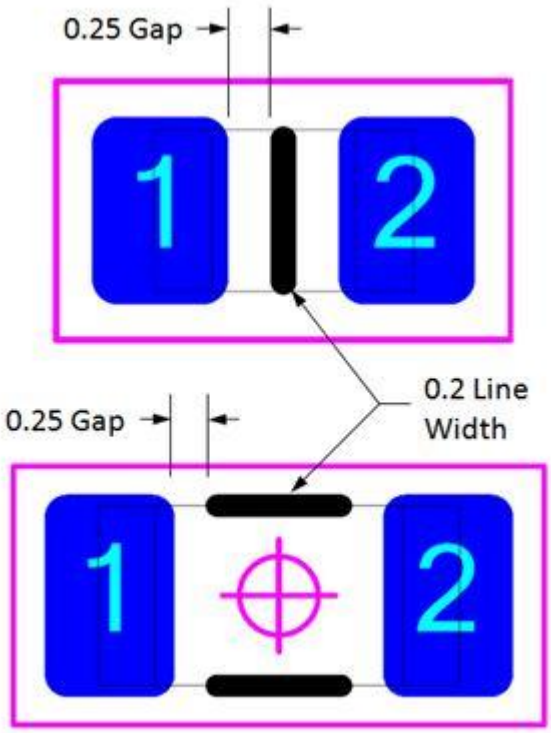


Figure 7. Two options available for standard non-polarized chips.

Figure 8 shows the silkscreen outline for the chip diode. The chip diode also features a post-assembly inspection dot so you can visually verify if the assembly inserted the diode or LED in the correct rotation. The polarized chip capacitor would have the same exact silkscreen outline but without the 0.6 mm bar.

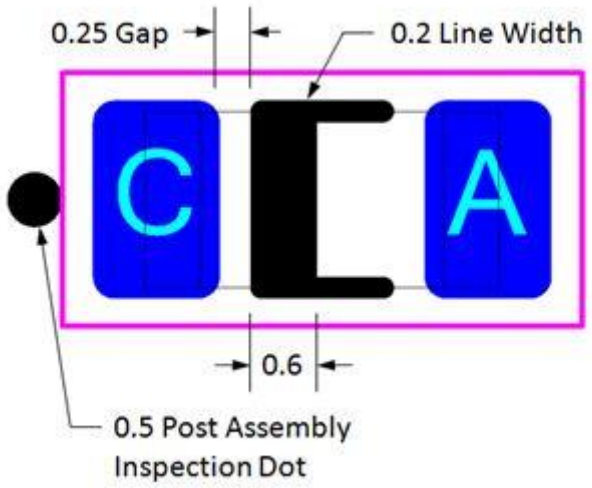


Figure 8. Silkscreen outline for the chip diode, showing the post-assembly inspection dot.

The assembly drawing outlines and polarity markings are totally different than the silkscreen outlines and polarity markings. The first most obvious difference is that the outline shape is 1:1 scale of the component body. This outline can be either the “Nominal” or “Maximum” component body size. Another difference is the reference designator is centered inside the component outline and is never moved or relocated. The reference designator default size is 1.5 mm height with a 10% line width.

The reference designator and assembly outline only change rules for micro-miniature parts. The assembly outline will grow as large as the placement courtyard in order to fit the reference designator inside the assembly outline. When the component gets smaller, the reference designator will decrease from the default 1.5 mm height to a sliding scale of values until it fits inside the assembly outline. The reference designator scaling width is always 10% of the height. The various reference designator heights for micro-miniature components are:

1.5 mm

1.25 mm

1.0 mm

0.75 mm

0.5 mm (this is the smallest human readable text height)

In Figure 9, the non-polarized and polarized capacitor, diode and resistor assembly outlines and reference designators are illustrated. Notice the absence of land pads. From all chip and molded body components, the land is removed from the SMT padstack to insure that the reference designators are unobstructed. Also, for CAD tools that have this feature, right reading orthogonal is always recommended so when the component is rotated, the reference designator is always flipped to right reading orientation.

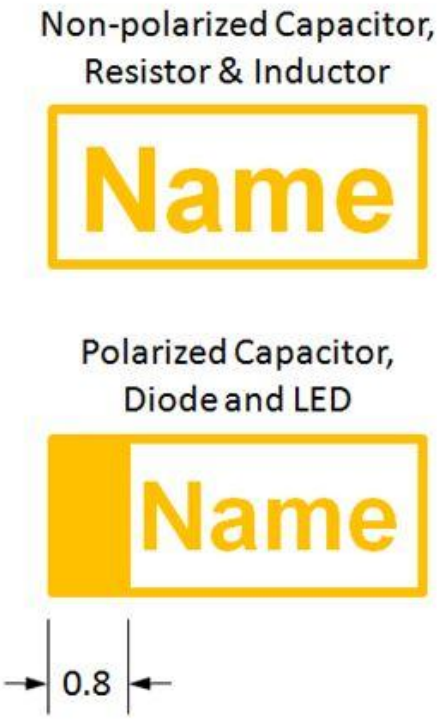


Figure 9. Graphic depicting non-polarized and polarized capacitor, diode and resistor assembly outlines and reference designators.

Molded Body Components

The next-most popular component family on a PCB design layout is the molded body tantalum capacitor (CAPM). The CAPM components have an “L-bend” component lead form. Most molded body tantalum capacitors are metric by default, including their standard EIA names:

3216 – 3.2 mm x 1.6 mm

6032 – 6.0 mm x 3.2 mm

7343 – 7.3 mm x 4.3 mm

Figure 1 illustrates the 6032 component and land pattern dimensions. I broke one rule to create this land pattern. Instead of a 1.0 mm land placement round-off I used a 2.0 mm land placement round-off to snap the land centers on a 0.5 mm grid from the center of the land pattern. When the land pattern is placed on a 0.5 mm grid, the land centers fall on a 0.5 mm grid. This improves the via fanout seen in Figure 3.

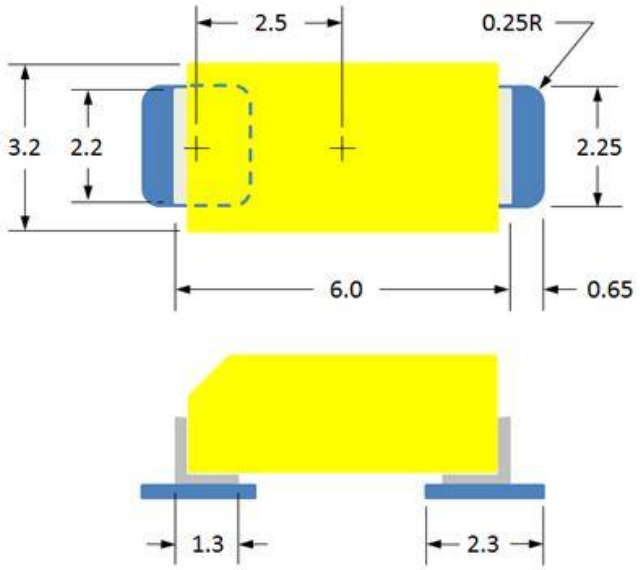


Figure 1. The 6032 component and land pattern dimensions.

Figure 2 shows the silkscreen and placement courtyard rules and sizes. The illustration shows the component leads on top of the land for graphic representation.

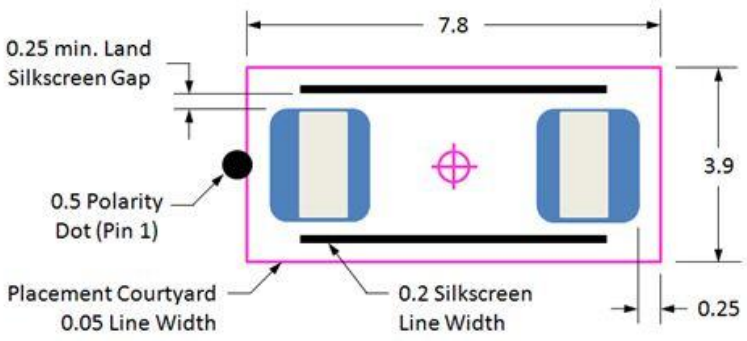


Figure 2. The silkscreen and placement courtyard rules and size.

The via fanout for a 6032 tantalum capacitor is shown in Figure 3. If you are going to use the same size via to maintain trace/space compatibility with the rest of the PCB layout I recommend at least two vias. The placement of these vias is critical in accomplish reduced impedance and increased capacitance. It's important that the vias be placed as close as possible to the capacitor terminal leads.

In Figure 3, the two vias exiting the side are 0.15 mm away from the terminal lead. The vias coming out the ends on the land pattern are 0.75 mm away from the terminal leads. That's five times further away than the vias coming out the sides; however, some engineers will request all four vias. Since all the traces and vias are snapped to a 0.5 mm grid, this makes copy/paste much easier when manually designing fanout of the 6032 molded body capacitors. The dot grid display is 1.0 mm and the land pattern is placed on a 0.5 mm grid. All the vias in this illustration fall on a 1.0 mm snap grid.

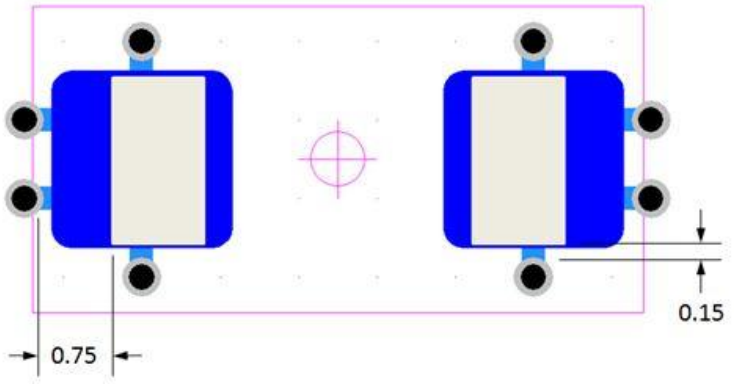


Figure 3. The via fanout for a 6032 tantalum capacitor.

See Figure 4 for the 7343 molded body tantalum capacitor. I recommend a larger via size with a 1.0 mm land size, 0.55 mm hole size, and 1.3 mm plane anti-pad. This via can carry more current and you only need two (but the EE will ask for a third one). The illustration in Figure 4 snaps all the vias to a 1.0 mm grid system. These vias are twice the size of the previous vias but all the same trace/space rules apply. The display grid is 1.0 mm.

Because the land pattern, traces and the vias are on a 1.0 mm snap grid, this improves the copy/paste feature for manual fanout of all of the 7343 molded body components in your PCB layout.

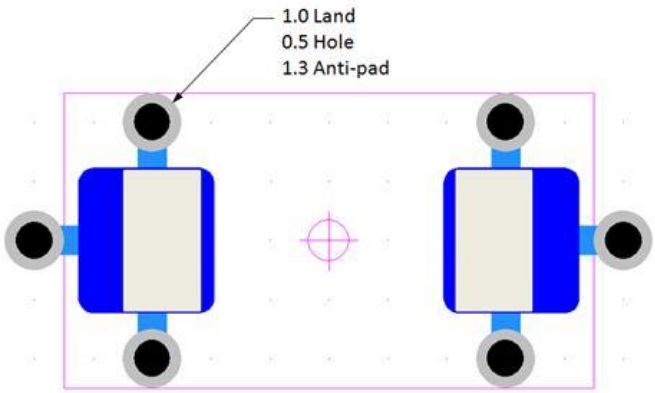


Figure 4. Graphic depicting the 7343 molded body tantalum capacitor.

SOT23 Components

The SOT23 is the most popular of the SOT component families. It features 3-, 5-, 6- and 8-pin variations and three popular pin pitches. Note: All pictures are shown in the “Nominal Environment” land pattern.

Figure 1 illustrates 0.5 mm pitch SOT23 3-pin and 8-pin examples.

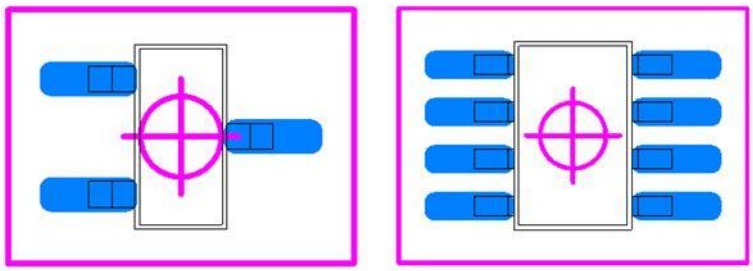


Figure 1. Graphic showing 0.5 mm pitch SOT23 3-pin and 8-pin examples.

0.5 mm Pitch SOT23 Fanout Examples

Figure 2 illustrates four different 0.5mm pitch 3-pin SOT23 land pattern via fanout techniques. The SOT23 parts are placed on a 0.5 mm grid system and all the vias snap to a 1.0 mm grid.

There are two 0.1 mm trace/space technology on all layers.

Via land size is 0.5 mm, hole size is 0.25 mm and plane anti-pad is 0.7mm

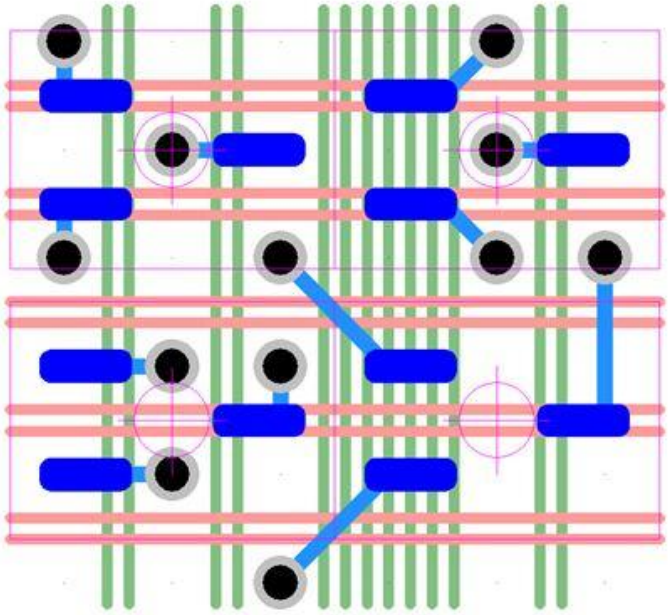


Figure 2. Four different 0.5mm pitch 3-pin SOT23 land pattern via fanout techniques.

0.5 Mm Pitch SOT23 Fanout Examples

Figure 3 illustrates four different 0.5mm pitch 8-pin SOT23 land pattern via fanout techniques. The SOT23 parts are placed on a 0.5 mm grid system and all the vias snap to a 1.0 mm grid. This allows two 0.1 mm trace/space technology on all layers.

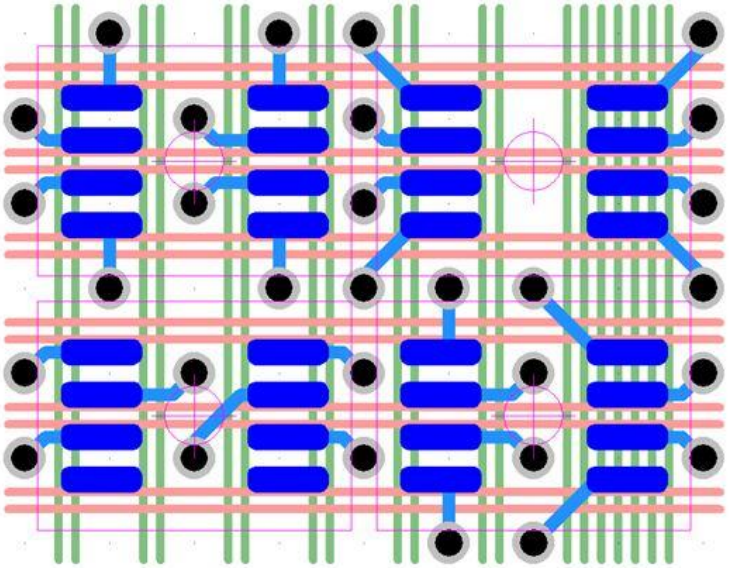


Figure 3. Four different 0.5mm pitch 8-pin SOT23 land pattern via fanout techniques.

Figure 4 illustrates 0.65 mm pitch SOT23 3-, 5-, 6- and 8-pin examples.

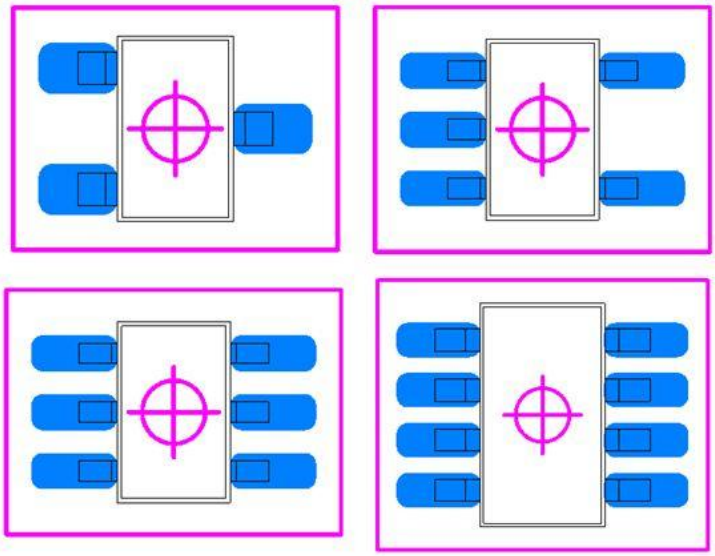


Figure 4.

0.65 mm Pitch SOT23 Fanout Examples

Figure 5 illustrates five different 0.65mm pitch 3-, 5-, 6- and 8-pin SOT23 land pattern via fanout techniques. The SOT23 parts are placed on a 0.5 mm grid system and all the vias snap to a 1.0 mm grid. This allows two 0.1 mm trace/space technology on all layers with 0.5 mm via land.

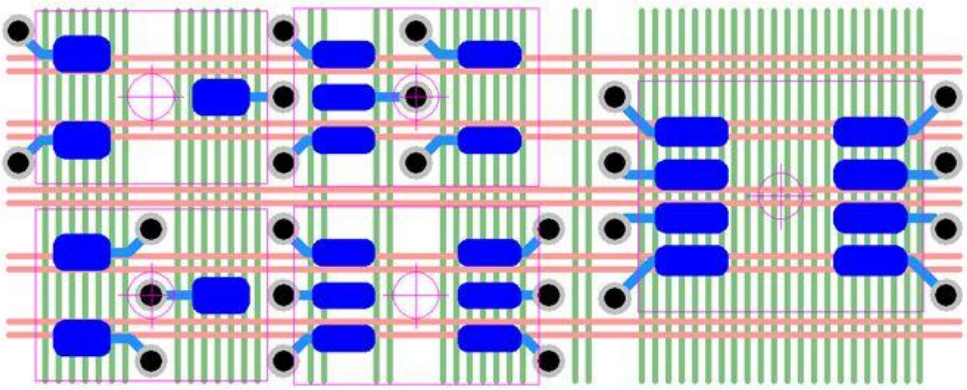


Figure 5.

Figure 6 illustrates 0.95 mm pitch SOT23 3-, 5-, 6- and 8-pin examples.

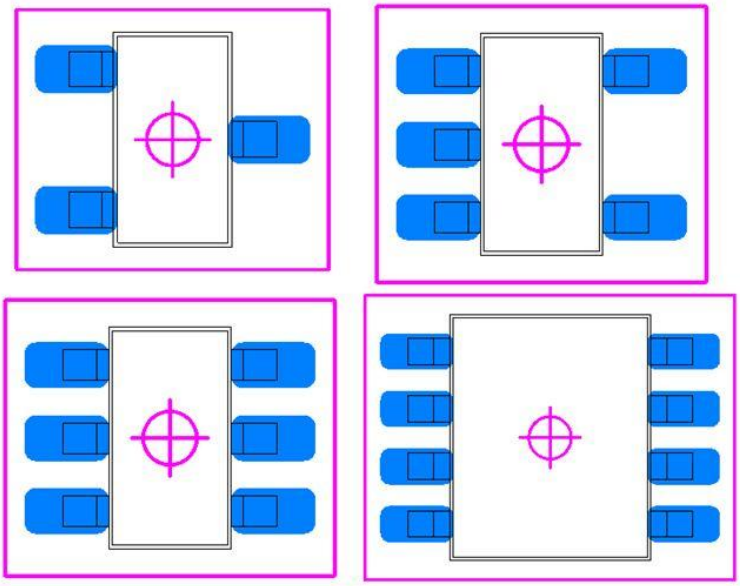


Figure 6.

0.95 mm Pitch SOT23 Fanout Examples

Figure 7 illustrates seven different 0.95mm pitch 3-, 5-, 6- and 8-pin SOT23 land pattern via fanout techniques. The SOT23 parts are placed on a 0.5 mm grid system and all the vias snap to a 1.0 mm grid. This allows two 0.1 mm trace/space technology on all layers.

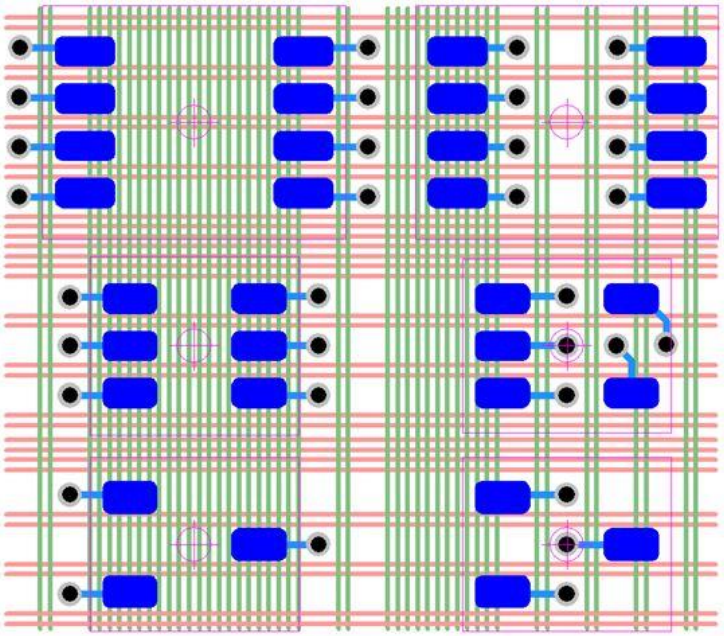


Figure 7. Seven different 0.95mm pitch 3-, 5-, 6- and 8-pin SOT23 land pattern via fanout techniques.

The SOT component family uses a gull wing component lead. All gull wing leaded components have four different sets of land pattern rules. These examples are for the “Nominal Environment”.

Pin pitch less than 0.625mm (side goal is -0.02 mm) considered “fine pitch”

Pin pitch greater than 0.625 mm (side goal is 0.03 mm)

Outward flat ribbon with pin pitch less than 0.625mm (heel goal is 0.15 mm and side goal is -0.02 mm)

Outward flat ribbon with pin pitch greater than 0.625mm (heel goal is 0.15 mm and side goal is 0.03 mm)

The formula that calculates the difference between gull wing and outward flat ribbon (mini gull wing) is shown in Figure 8.

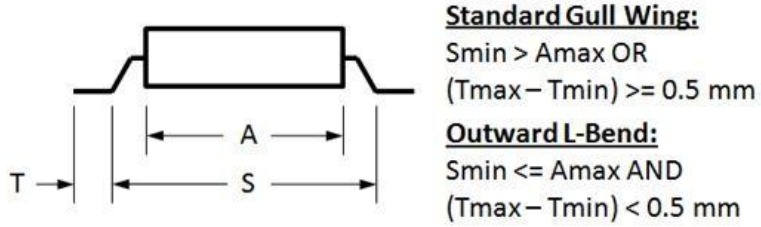


Figure 8. Formula that calculates the difference between gull wing and outward flat ribbon.

We already discussed chip and molded body assembly outlines and ref des in the last column. It’s important to note that the lands (pads) do not get added to the assembly drawing layer for small parts. The two most important things on the assembly drawing are the Ref Des and Component Outline. If the

part is too small and the lands interfere with the Ref Des, then do not add the top assembly lands to the padstack. However, if the lands do not interfere with the Ref Des then we should add the top assembly lands to the padstack.

Here are some of the various assembly outlines for the 0.95 mm pitch SOT23 component family. See Figure 9 for the 3-, 5- and 6-pin versions of the assembly outline, Ref Des, polarity marker for pin 1 location and lands (pads).

Figure 9. Silkscreen outlines for the various SOT component families.

There are a number of silkscreen outlines for the various SOT component families; Figure 9 illustrates several of them. See Figure 10 for the SOT23 silkscreen outline, polarity marker and 0.5 mm post-assembly inspection dot for pin 1 location and lands (pads). In this case the silkscreen outline is too narrow for an adequate polarity marker inside the outline, so the post assembly inspection dot for pin 1 will have to be sufficient.

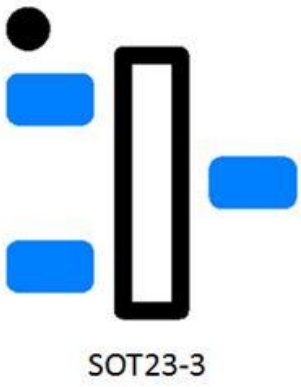


Figure 10. Silkscreen outline, polarity marker and 0.5 mm post-assembly inspection dot.

SOT223 Components

The SOT223 is the second-most popular part in the small outline transistor (SOT) component families. The SOT223 comprises 4-, 5- and 6-pin variations as well as three popular pin pitches, which include 1.27 mm, 1.50 mm and 2.30 mm pitch. Figure 1 shows the 6-pin 1.27 mm pitch SOT223 land pattern. The particular land pattern shown is portrayed in the Nominal Environment.

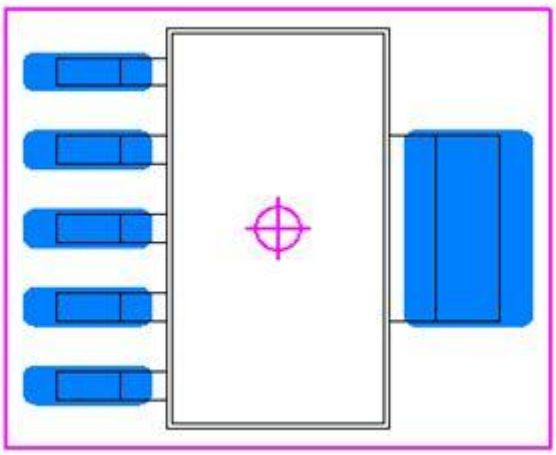


Figure 1: SOT 223 with 1.27 mm pitch (Nominal Environment).

Figure 2 shows the 6-pin 1.27 mm pitch SOT223 land pattern via fanout. This fanout uses a power via with a 1.00 mm land and a 0.50 mm hole snapped to a 1.00 mm grid. The signal trace/space rules are for this layout are 0.10 mm.

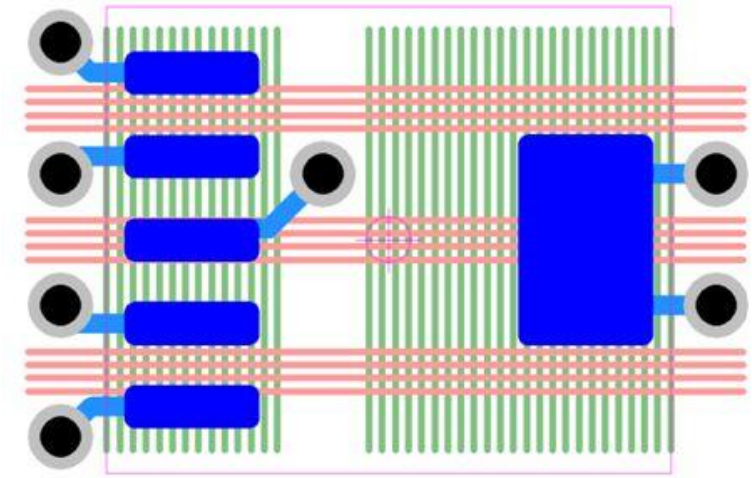


Figure 2: 6-pin, 1.27 mm fanout.

Figure 3 shows the 5-pin 1.50 mm pitch SOT223 land pattern.

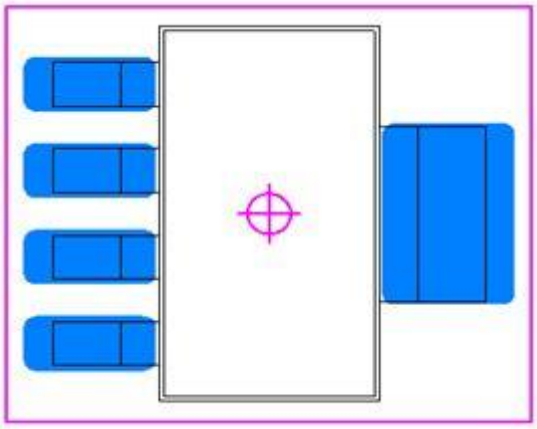


Figure 3. 5-pin 1.50 mm pitch land pattern.

Figure 4 shows the 5-pin 1.50 mm pitch SOT223 land pattern via fanout. This layout also uses a power via with a 1.00 mm land and a 0.50 mm hole snapped to a 1.00 mm grid. The trace/space rules are also 0.10 mm.

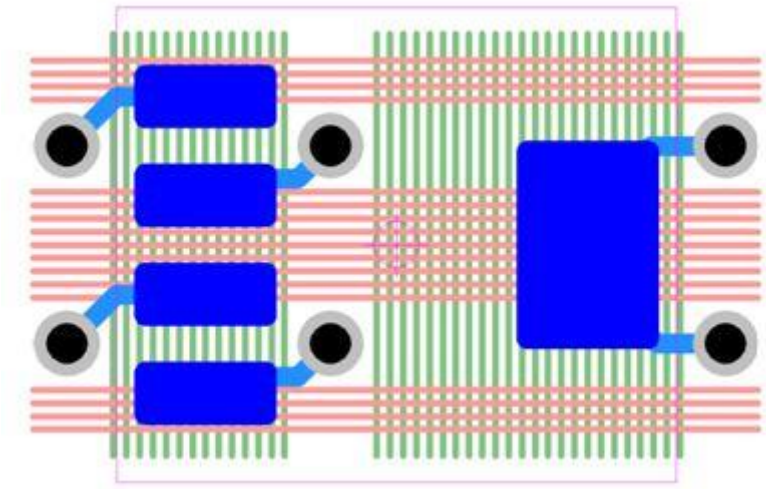


Figure 4: 5-pin, 1.50 mm pitch fanout.

Figure 5 shows the 4-pin 2.30 mm pitch SOT223 land pattern. Figure 6 shows the 4-pin 2.3 mm pitch SOT223 land pattern via fanout using the same power and trace/space rules as the previous examples.

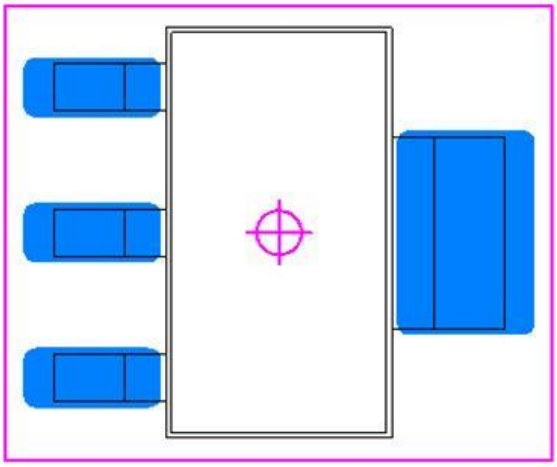


Figure 5: 4-pin, 2.30 mm pitch land pattern.

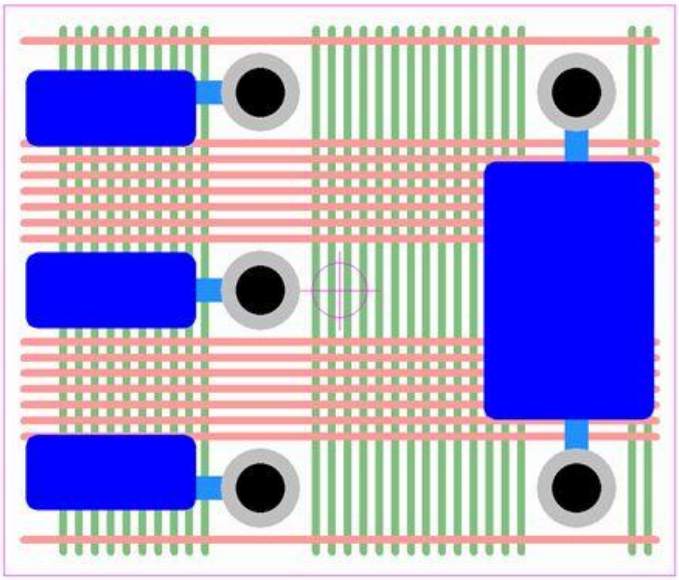


Figure 6: 4-pin, 2.30 mm pitch fanout.

Component Leads

The SOT223 component family uses a “gull wing” component lead. All gull wing leaded components have four different sets of land pattern rules. These example rules are for the Nominal Environment:

Pin pitch less than 0.625 mm (side goal is -0.02 mm) considered “fine pitch.”

Pin pitch greater than 0.625 mm (side goal is 0.03 mm).

Outward flat ribbon with pin pitch less than 0.625 mm (heel goal is 0.15 mm and side goal is -0.02 mm).

Outward flat ribbon with pin pitch greater than 0.625 mm (heel goal is 0.15 mm and side goal is 0.03 mm).

The formula that calculates the difference between gull wing and outward flat ribbon is shown in Figure 7.

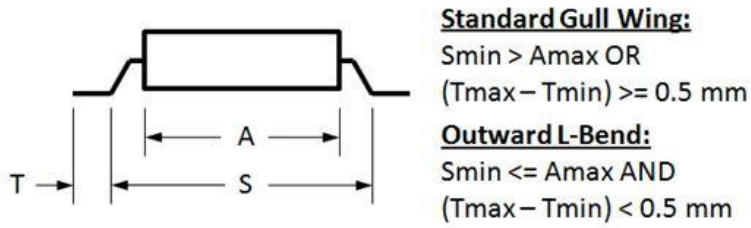


Figure 7: Dimensions for standard gull wing vs. outward L-bend.

We've already discussed chip and molded body assembly outlines and ref des. It's important to note that the lands (pads) do not get added to the assembly drawing layer for small parts. The two most important items on the assembly drawing are the ref des and component outline. If the part is too small and the lands interfere with the ref des, then do not add the top assembly lands to the padstack. However, if the lands do not interfere with the ref des, then add the top assembly lands to the padstack.

Here are some of the various assembly outlines for the SOT223 component family. See Figure 8 for the 4-, 5- and 6-pin versions of the assembly outline, ref des, and polarity marker for pin 1 location and lands (pads).

Figure 8: Assembly outlines for 4-, 5- and 6-pin SOT223.

Figure 9 illustrates some of the various silkscreen outlines for the SOT component families, including the SOT223 version of the silkscreen outline, polarity marker and 0.50 mm post-assembly inspection dot for pin 1 location and lands (pads).

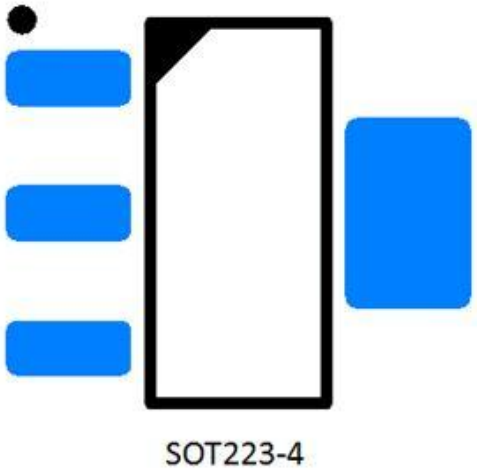


Figure 9: 4-pin example silkscreen outline.

SOT143 and SOT343 Components

After the SOT223, the next-most popular small outline transistors (SOT) component families are the SOT143 and SOT343. Both families have four pins, with a larger Pin 1. The pin pitch is 1.90 mm.

SOT143 Family

There are three different pin configurations for the SOT143 package: Pin 1 is wide pin on upper left, Pin 1 is wide pin on upper right (reverse pin order), and the third has Pin 2 as a wide pin on lower left (custom). Figure 1 illustrates all three of these patterns.

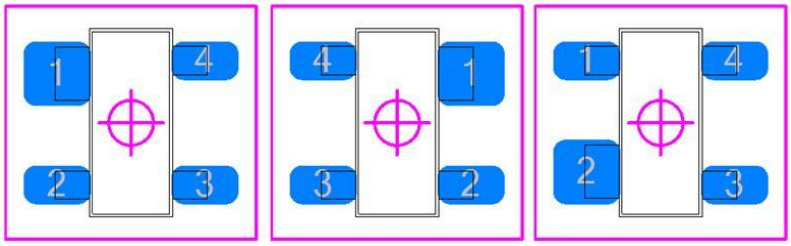


Figure 1: The three pin 1 configurations for the SOT143.

Figure 2 shows the 4-pin 1.90 mm pitch SOT143 land pattern via fanout using a via with a 0.50 mm land and a 0.25 mm hole snapped to a 1.00 mm grid. The trace/space rules are 0.10 mm and the routing grid is 0.10 mm.

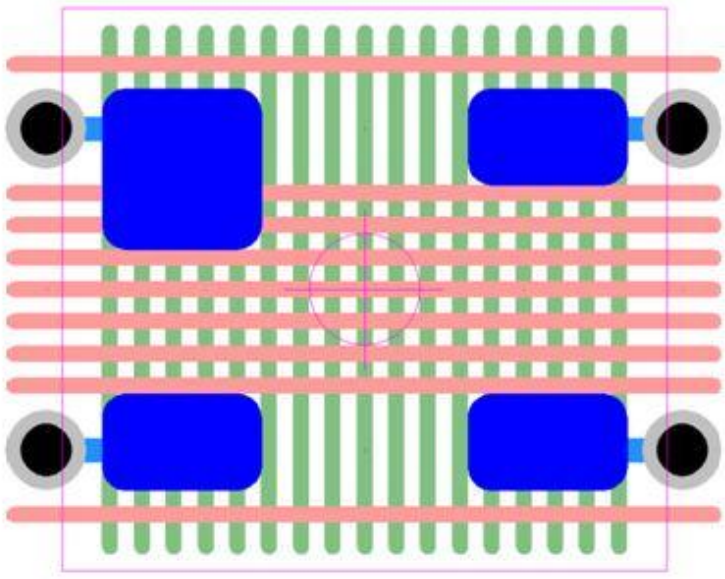


Figure 2: SOT143 via fanout.

SOT343 Family

The SOT343 is the next most popular component family. This family of components also has four pins, with Pin 1 always in the upper left quadrant. Pin 1 is also wider than the other three pins. See Figure 3.

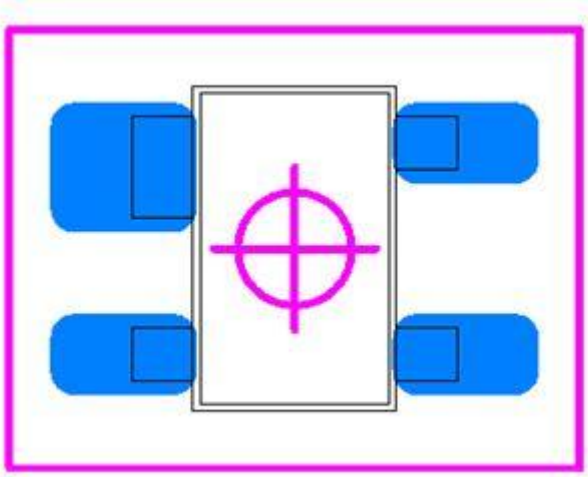


Figure 3: Land pattern for the SOT343 family.

Figure 4 shows the 4-pin 1.30 mm pitch SOT343 land pattern via fanout using a via with a 0.50 mm land and a 0.25 mm hole snapped to a 1.00 mm grid. Like the SOT143, the trace/space rules are 0.10 mm and the routing grid is 0.10 mm. The via fanout direction depends on which layer you need more routing channels.

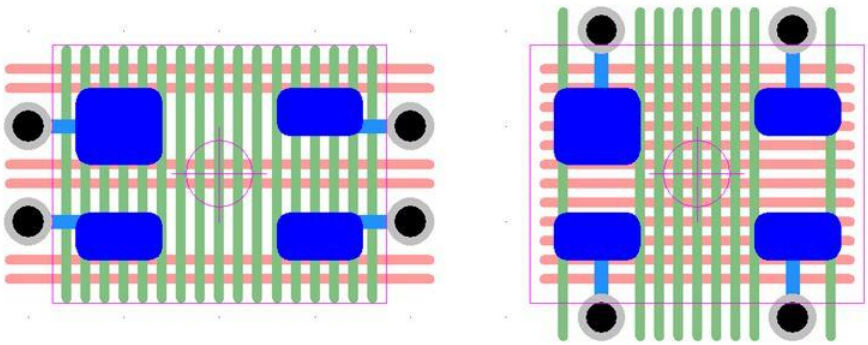


Figure 4: SOT343 fanout.

Component Leads

Both the SOT143 and SOT343 component families use a gull-wing component lead. All gull-wing leaded components have four different sets of land pattern rules. These rule examples are for the “Nominal Environment.”

Pin pitch less than 0.625 mm (side goal is -0.02 mm) considered “fine pitch.”

Pin pitch greater than 0.625 mm (side goal is 0.03 mm).

Outward flat ribbon with pin pitch less than 0.625 mm (heel goal is 0.15 mm and side goal is -0.02 mm).

Outward flat ribbon with pin pitch greater than 0.625 mm (heel goal is 0.15 mm and side goal is 0.03 mm).

The formula that calculates the difference between gull-wing and outward flat ribbon (mini gull-wing) is shown in Figure 5.

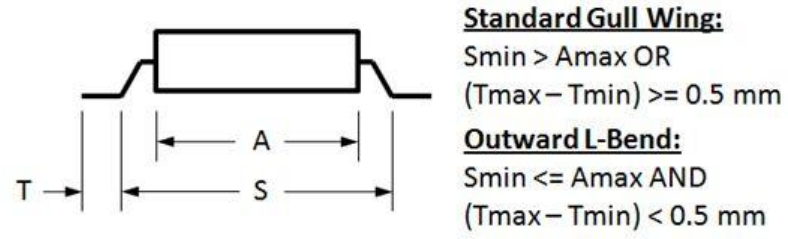


Figure 5: Dimensions for standard gull-wing and outward L-bend leads.

We already discussed chip and molded body assembly outlines and ref des. It's important to note that the lands (pads) do not get added to the assembly drawing layer for small parts. The two most important aspects of the assembly drawing are the ref des and component outline. If the part is too small and the lands interfere with the ref des, then do not add the top assembly lands to the padstack. However, if the lands do not interfere with the ref des, then we should add the top assembly lands to the padstack.

Figure 6 illustrates some of the assembly outlines for the SOT143 component family showing both standard and reverse pin versions of the assembly outline, ref des, polarity marker for pin 1 location and lands (pads).

Figure 6: Assembly outlines for SOT143.

Figure 7 illustrates some of the various silkscreen outlines for the SOT component families. These include the SOT143 version of the silkscreen outline, polarity marker and 0.5 mm post-assembly inspection dot for pin 1 location and lands (pads).

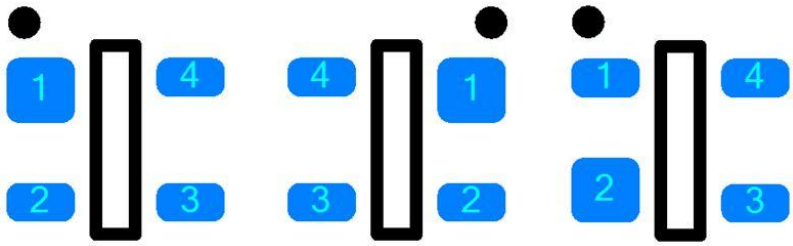


Figure 7: Silkscreen for SOT143 components.

BGA Components

The ball grid array, commonly known as the BGA, has been around since the 1980s. The pin pitch began at 1.50 mm and then quickly went to 1.27 mm (50 mils), where it held steady for about 15 years. Then in the late 1990s, the 1.00 mm pitch BGA was introduced. Every few years since then, the pin pitch has dropped. Today 0.40 mm pitch BGAs are in every cell phone and 0.30 mm pitch BGAs are the next generation. Figure 1 shows the lead type for this component family.

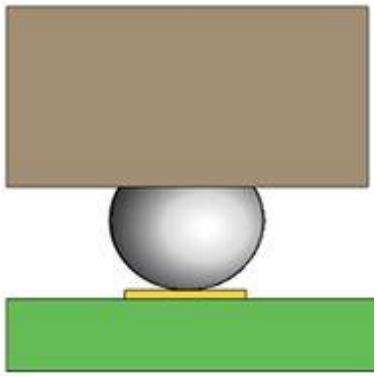


Figure 1. BGA leads — a lead ball collapsed against the PCB land.

Ball grid array components can have one of two types of ball leads:

Non-collapsing - this is normally employed for 0.50 mm pitch and smaller BGAs, where the land (pad) is larger than the ball to allow for via-in-pad technology and to provide an adequate annular ring. The solder mask can be the same size as the land with non-collapsing balls. In some cases, the land for fine pitch BGAs is solder-mask defined where the solder mask encroaches slightly over the land. This provides protection for any trace routing between the lands but the most significant benefit is to help secure the land to the PCB. During cell phone "drop testing", the BGA solder joint normally holds better than the land to the Prepreg. i.e.: drop tests prove that the non-solder-mask land will rip from the PCB before the solder joint breaks. So the solder-mask defined land is secured better to the PCB for drop testing.

Collapsing - this is normally 0.65 mm pitch and larger, where the land (pad) is smaller than the ball size to allow the ball to collapse around the sides of the land. This requires a non-solder-mask-defined land where the solder mask must be larger than the land.

Figure 2 illustrates examples of non-collapsing and collapsing BGA balls.

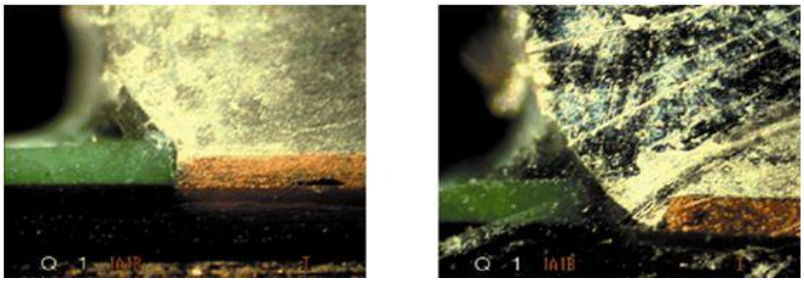


Figure 2. Non-collapsing ball (left) and collapsing ball (right) BGAs, highly magnified.

The BGA land (pad) size is determined by the ball size as seen below in Table 1, from the IPC-7351B land pattern standard. Notice the correlation between the "reduction" and the "land pattern density level." The three density levels change the land size reduction percentage, but they also determine the placement courtyard excess (See Table 3).

Nominal Ball Diameter	Reduction	Land Pattern Density Level	Nominal Land Diameter	Land Variation
0.75	25%	A	0.55	**0.60** - 0.50
0.65	25%	A	0.50	**0.55** - 0.45
0.60	25%	A	0.45	**0.50** - 0.40
0.55	25%	A	0.40	**0.45** - 0.35
0.50	20%	B	0.40	**0.45** - 0.35
0.45	20%	B	0.35	**0.40** - 0.30
0.40	20%	B	0.30	**0.35** - 0.25
0.35	20%	B	0.30	**0.35** - 0.25
0.30	20%	B	0.25	**0.25** - 0.20
0.25	20%	B	0.20	**0.20** - 0.17
0.20	15%	C	0.17	**0.20** - 0.14
0.17	15%	C	0.15	**0.18** - 0.12
0.15	15%	C	0.13	**0.15** - 0.10

Table 1. Land approximation (mm) for collapsible solder balls.

Note: The IPC-7351B LP Calculator uses this chart for calculations

It is very important to note that IPC prefers the Maximum Material Condition for all BGA Land sizes; IPC does not use the Nominal Land Diameter, but instead uses the Maximum Land Variation Diameter (notice the bold numbers in the chart's land variation column). The standard ball sizes are in 0.05 mm increments until the pin pitch hits 0.50 mm or less. However, even though the world standards organizations try to keep BGA balls sizes in 0.05 mm increments, component manufacturers sometimes do not adhere to the standard and create BGA ball sizes in 0.01 mm increments.

But I have never seen a BGA ball size less than a 0.01 mm increment. Also, the BGA pin pitches are in 0.05 mm increments. As a result, the BGA land (pad) sizes are in 0.05 mm increments, including the via fanout padstacks and hole sizes.

IPC-7351B features a three-tiered BGA formula for placement courtyard excess that uses the BGA ball size to calculate an adequate placement courtyard for BGA rework tools. If the BGA has a large ball size, larger rework equipment is necessary to unsolder the increased solder volume.

With a small ball size, the placement courtyard can be smaller because less heat is then required to unsolder the BGA component for rework. However, the end-user may not plan to rework the BGA if it fails. In that case, there is no need to have a robust placement courtyard, but a recommended minimum placement courtyard excess is 0.5 mm.

Non-Collapsing Ball BGA Components

Table 2 shows land size calculations for non-collapsing BGA balls.

Nominal Ball Diameter	Increase	Nominal Land Diameter	Land Variation
0.75	15%	0.85	**0.90** - 0.80
0.65	15%	0.75	**0.80** - 0.70
0.60	15%	0.70	**0.75** - 0.65
0.55	15%	0.65	**0.70** - 0.60
0.50	10%	0.55	**0.60** - 0.50
0.45	10%	0.50	**0.55** - 0.45
0.40	10%	0.45	**0.50** - 0.40
0.35	10%	0.40	**0.45** - 0.35
0.30	10%	0.35	**0.40** - 0.30
0.25	10%	0.30	**0.35** - 0.25
0.20	5%	0.21	**0.26** - 0.16
0.17	5%	0.18	**0.22** - 0.13
0.15	5%	0.16	**0.21** - 0.11

Table 2. Non-collapsing BGA ball land calculations.

Figure 3 is a 0.50 pitch non-collapsing BGA ball. Instead of shrinking, the non-collapsing land size gets larger to handle the solder volume that creates the solder joint. This technology is new to the electronics industry and was created as a solution for lead-free BGA balls and via-in-pad technology as a routing solution for fine pitch BGA components.

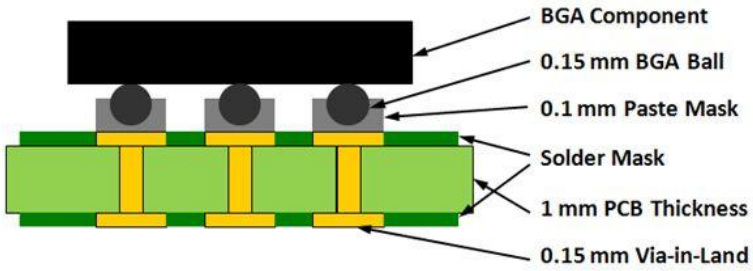


Figure 3. Non-collapsing 0.5 mm pitch BGA.

Via-in-Land Technology	Trace/Space & Grid Data
BGA Ball Size: 0.15	Trace Width: 0.075
BGA Land Dia: 0.275	Trace/Trace Space: 0.075
Hole Size: 0.15	Trace/Via Space: 0.075
Thermal Relief Required	Trace/BGA Land: 0.075
Plane Clearance: 0.425	Routing Grid: 0.05
Solder Mask: 1:1 scale	Part Place Grid: 1

IPC-7351A has a three-tiered BGA formula for placement courtyards that uses the BGA ball size to calculate an adequate placement courtyard for BGA rework tools.

If the BGA has a large ball size, larger rework equipment is necessary to unsolder the large solder volume. With a small ball size, the placement courtyard can be smaller as less heat is then required to unsolder the BGA component for rework. However, the end user may not plan to rework the BGA if it fails. In that case, there is no need to have a robust placement courtyard.

Table 3 below represents the three-tiered scenario and the different placement courtyard excess size determination.

Lead Part	Most Density Level A	Nominal Density Level B	Least Density Level C
Collapsing Ball	25% Reduction	20% Reduction	15% Reduction
Non-collapsing Ball	15% Reduction	10% Reduction	5% Reduction
Courtyard Excess	**2.00**	**1.00**	**0.50**
Round-off Factor	Round off to the nearest two place 0.05 decimal, i.e.: 1.00, 1.05, 1.10, 1.15		

Table 3. BGA density levels for placement courtyard size determination.

SMD Bottom and Flat Lead Forms

Before we go deeper into the various component families, we need to clarify the component lead forms of today's component packaging technology: What is going to be eventually phased out, what is new and why. This is Part 1 of 2 columns on component lead forms. Part 2 will cover side and bent leads.

The pin (component lead) pitch and the overall body height are continually shrinking. This is why the SSOP and TSOP land pattern names have to be dropped from the standard. In this nomenclature, S = Shrink for fine pitch and T = Thin for low profile height.

If these two values are constantly changing, then where is the line drawn? Whose part is thin or fine pitch, and by what measure? The gull-wing lead has hit the limit at 0.40 mm pitch. Most assembly shops will try to convince you to swap that part out of your design for a larger pin pitch. However, no-lead SON and QFN lead styles are being produced and manufactured at 0.40 mm pitch with no problems. The finer-pitch parts have more I/Os and a smaller footprint with a much lower profile than J-lead or gull-wing packages, so it's obvious that the component industry is going to be no-lead or bottom-only flat-lead or side-lead packages.

Let's review the bottom-only and flat-component lead forms. The BGA has been around since the 1980s but the pin pitch started out with 1.50 mm and then quickly went to 1.27 mm (50 mils) for about 15 years. Then in the late 1990s, the 1.00 mm pitch BGA was introduced and every couple years a smaller pin pitch was introduced. Today 0.4 mm pitch BGAs are in every cell phone and 0.3 mm pitch BGAs are the next generation. See Figure 1.

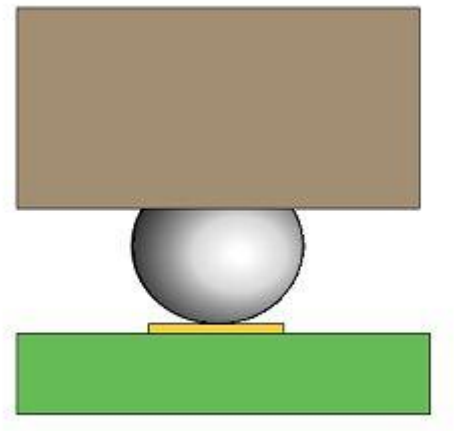


Figure 1. BGA ball-to-land illustration.

For more information about BGAs, read my white paper
"Metric Pitch BGA and Micro BGA Routing Solutions."

The next lead form in the bottom-only category is the "bump" lead. This is widely used in a package called land grid array or LGA. The land (pad) size can be the same as the maximum bump lead diameter. Via-in-pad technology can be much more forgiving with the bump lead than BGA voids due to a dimple in the land after the plug and plate process. This lead form is also highly compatible with lead-free solder. See Figure 2.

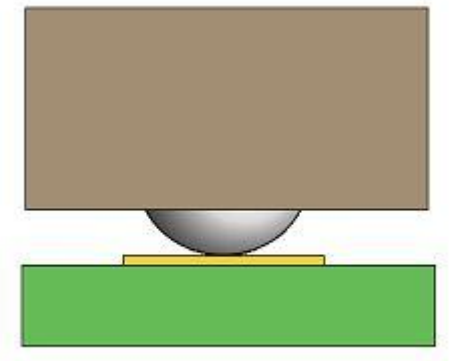


Figure 2.

The next grid array lead form is the bottom flat, which is also used in LGA component packages. Linear Technologies is the leading provider of bottom flat lead LGA packages. This lead form is also highly compatible with lead-free solder alloys as there is no requirement for wetting (flow) properties in the solder.

The other flat no-lead is referred to as a "pull-back" or "bottom-only" lead. We can also categorize the pull-back lead small outline no-lead (SON) and quad flat no-lead (QFN) component packages with this solder joint goal, as a slight periphery land is required to allow the solder to move from under the lead to the periphery to surround the protruding lead for a solid solder joint.

The solder joint goal is a periphery land around the terminal. Pull-back or bottom-only leads come in three lead shapes:

D-Shape (or vullet in some CAD tools)

Square

Rectangle

This lead style has the same solder joint goals as the bottom-only “bump” LGA lead. See Figure 3.

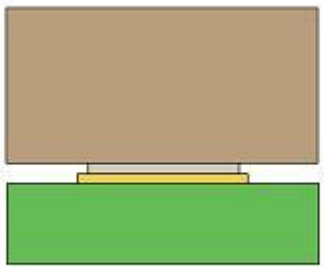


Figure 3.

The next grid array component lead is the "column." Actel and Xilinx are the leading manufacturers of this lead style. You will not find any pin pitches smaller than 1.00 mm for the column lead. The land must be slightly larger than the column to form a good solder joint. See Figure 4.

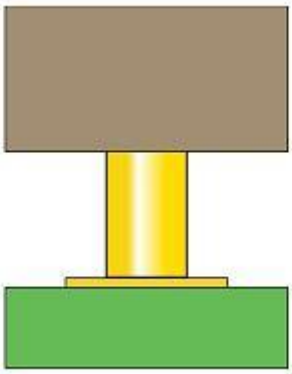


Figure 4.

The last SMT grid array is the newest lead form in the industry: the "pillar column." Recently introduced by Actel, this component lead has much promise for an improved solder joint. But time will tell how long this one will last. See Figure 5.

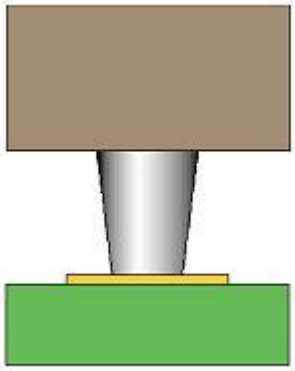


Figure 5.

Flat lead components are coming on strong. These are the SODFL (Small Outline Diode Flat Lead) 2-leaded components and the SOTFL (Small Outline Transistor Flat Lead) packages that come in 3-, 5-, 6- and 8-lead components. Both of these component families are the direct replacement for the gull-wing lead SOD and SOT-23 packages. See Figure 6.

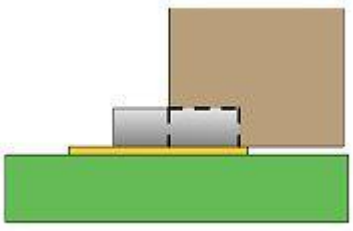


Figure 6.

Flat no-lead is used in the SON (Small Outline No-lead) with terminals on two sides and QFN (Quad Flat No-lead) with leads on four sides. The most common SON & QFN today is the "edge" lead, where the component lead starts under the component and goes out to the component body edge. This solder joint goal requires a toe, heel and side solder fillet where the toe joint is visible for inspection. See Figure 7.

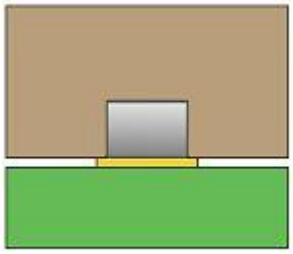


Figure 7

The flat thermal lead comes in a DPAK where the signal pins and gull-wing and thermal lead are flat. The flat thermal lead is also used as the heat sink for SON, QFN, SOP and QFP packages. It is usually embedded in the plastic component body and therefore the solder joint goals are usually 1:1 scale for the maximum component lead size and land size. See Figure 8.

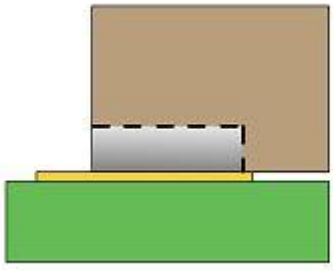


Figure 8

The last component lead form in the list is the "underbody outward L." This lead form is used for aluminum electrolytic capacitors and two-pin SMD crystals. This lead form has two different solder joint goals that are based on the component height. Once the component height exceeds 10 mm, the solder joint goals have to be more robust. See Figure 9.

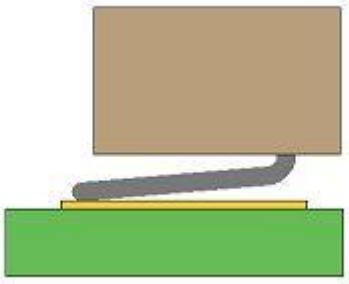


Figure 9

SMD Side and Bent Lead Forms

Recall in last week’s column, the pin (component lead) pitch and the overall body height are continually shrinking. This is why the SSOP and TSOP land pattern names have to be dropped from the standard: S = Shrink for fine pitch and T = Thin for low profile height. If these two values are constantly changing, where is the line drawn? Whose part is thin or fine pitch and by what measure? The gull-wing lead has hit the wall at 0.4 mm pitch.

Most assembly shops will try to convince you to swap that part out of your design for a larger pin pitch; however, no-lead SON and QFN lead styles are being produced and manufactured at 0.4 mm pitch with no problems. The finer-pitch parts have more I/Os and a smaller footprint with a much lower profile than J-lead or gull-wing packages, so it's obvious that the component industry is going to be no-lead or bottom only flat lead or side lead packages.

The "corner concave" lead form is primarily used for the oscillator component family. It's perfect for oscillators because it only has the four leads that are necessary for the standard oscillator requirements. See Figure 1.

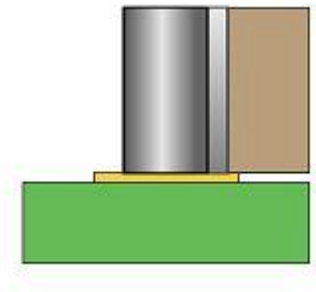


Figure 1.

The "cylindrical end cap" goes with the metal electrode lead face (MELF) component family for resistors and diodes. I just can't figure out why the industry still produces round components, but engineers continue to design them into their schematics. In some cases these components can easily roll off the workbench or circuit board before they have been soldered into place because of their cylindrical shape and small size. As such, there is a joke that suggests an alternate meaning for the acronym MELF: "Most End up Lying on Floor."

Mostly, this happens if the mechanical pressure of the SMD placer nozzle is too low. If the MELF resistors are placed into the solder paste with enough pressure this problem can be minimized. But be careful if SOD-80 glass diodes are used; those types are different compared to MELF resistors and the mechanical robustness is limited. See Figure 2.

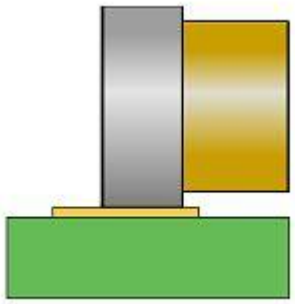


Figure 2.

Every PCB designer is familiar with the gull-wing lead (See Figure 3), but it has two separate rule sets that are defined by the pin pitch:

Less than 0.625 mm pitch (fine pitch)

Greater than 0.625 mm pitch

These component families include:

Ceramic flat package (CFP)

Ceramic quad flat package (CQFP)

Quad flat pack (QFP)

Small outline diode (SOD)

Small outline package (SOP)

Small outline transistor (SOT)

Transistor outline (TO)

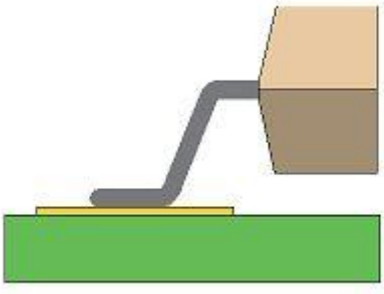


Figure 3.

The "inward flat ribbon L" is used for the molded body component family. This includes polarized and non-polarized capacitors, inductors, resistors and LEDs. The most popular is the tantalum capacitor. See Figure 4.

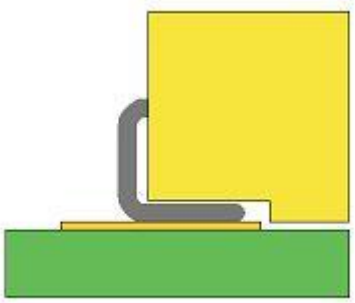


Figure 4.

The "J-lead" is one of the original SMT leads that became popular with the PLCC (plastic leaded chip carrier) and then the SOJ (small outline J-lead). This lead form was very popular because the leads were stable and easy to manually solder. And the solder joint was easy to inspect. However, with the advent of high speed technology, lead-free solder, low profile fine pitch component packages, this lead form will be one of the first SMT leads to become obsolete. See Figure 5.

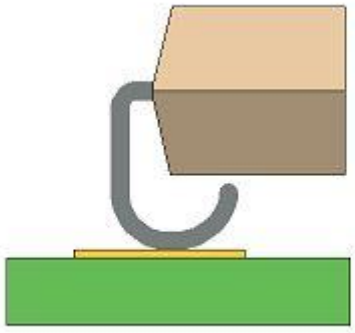


Figure 5.

The "outward flat ribbon L" lead is used to reduce the footprint size of SOT and SOP components. It's similar to a gull wing lead, but the lead bends downward immediately coming out of the component body and then is bent flat. The flat lead is very compatible with lead-free solder alloys and takes up less PCB real-estate. Since there is no heel and these components are so "low profile," the land is usually trimmed at the nominal component body. If the land (pad) protrudes under the component body, it will end up with solder on the bottom of the component during reflow. See Figure 6.

The outward L lead also has two separate rule sets that are defined by the pin pitch:

Less than 0.625 mm pitch (fine pitch)

Greater than 0.625 mm pitch

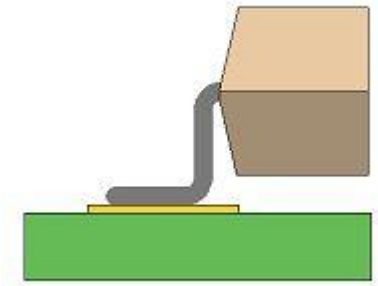


Figure 6.

The "rectangular end cap" is used for discrete resistors, capacitors, inductors and LEDs. This lead type is by far the most popular due to the component count. The rectangular end cap lead form makes up 80-90% of the total part quantity of the average PCB. These components are easy to manually solder and easy to rework if necessary. However, the new DFN (dual flat no-lead) component with bottom only terminations is better for lead-free solder and part placement density. See Figure 7.

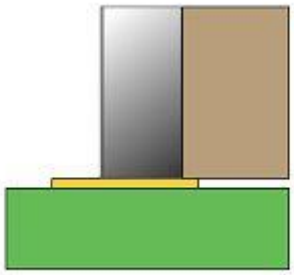


Figure 7.

The "side lead" comes in 3 different lead styles (See Figures 8, 9 & 10):

Concave

Convex

Flat

The side lead is on the outside perimeter of the component body and normally runs from the bottom to the top of the component. It is used widely for chip arrays and LCC (leadless chip carriers) and has 2 different sets of solder joint goals depending on the lead pitch:

Pitch is less than or equal to 1 mm

Pitch is greater than 1 mm

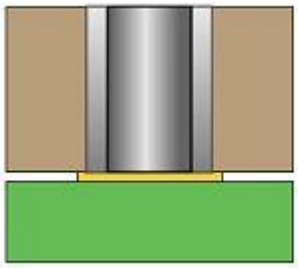


Figure 8. Concave side lead.

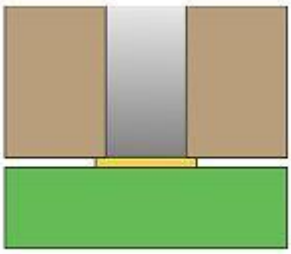


Figure 9. Flat side lead.

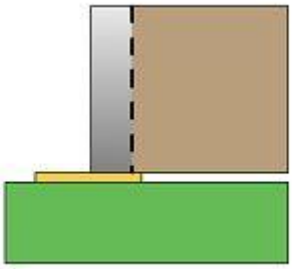


Figure 10. Convex side lead.

Now we have covered all the component lead forms. Next week, we'll dive into the various component families and relate their lead forms back to this post. It's going to be interesting to find out what new component lead will be invented by a component manufacturer in the years to come, but when they do, the IPC-7351 land pattern committee will be there to develop the optimized solder joint goal chart.

Placement Courtyards

The IPC-7351B standard focuses on five two major aspects of the CAD library:

1. Land (pad) size and spacing calculations
2. Placement courtyard excess boundary
3. Land pattern naming convention
4. Zero component orientation
5. Padstack naming convention

All of the other aspects of the CAD library section such as silkscreen and assembly outlines, polarity markings, reference designators, centroid marking, etc. are considered user-definable drafting items. This includes all of the rules that pertain to these items such as line widths, silkscreen to land spacing, polarity sizes, reference designator height, etc. They are not part of the IPC-7351B standard.

The placement courtyard boundary *is* defined in the IPC-7351B standard, but the line width used to create the closed polygon outline shape is user-definable. There are industry recommendations, like the IPC-2610 series for fabrication and assembly documentation. The IPC LP Calculator uses 0.05 mm as the default line width. The default solder mask and paste mask values are mentioned in the IPC-7351B as to be 1:1 scale of the land size, but this is only a recommendation.

See courtyard determination in Figures 1 and 2 below to see the three outlines defined by IPC-7351B as:

Maximum component boundary

Minimum placement courtyard

Courtyard manufacturing zone

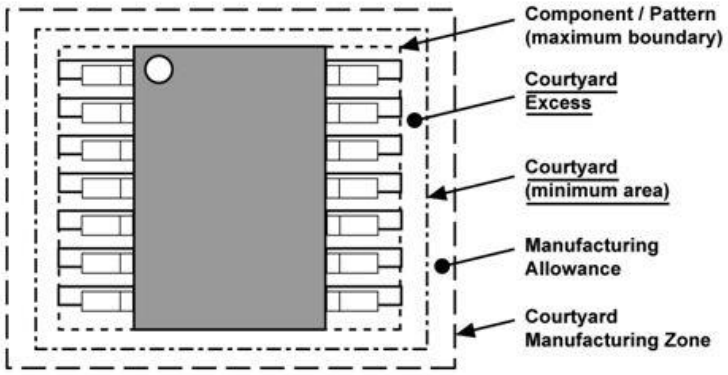


Figure 1. Plated through-hole courtyard excess determination.

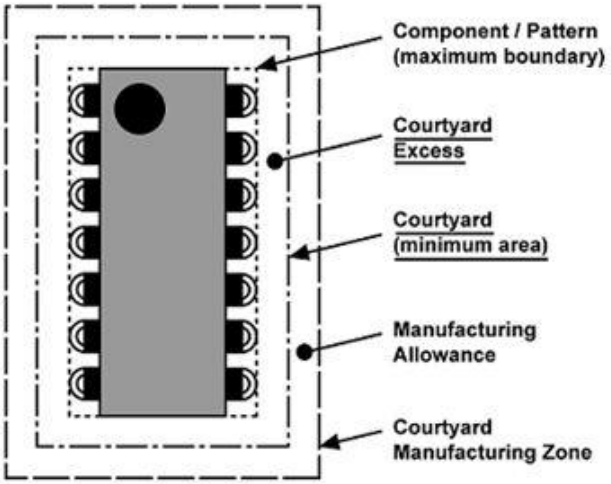


Figure 2. Plated through-hole courtyard excess determination.

Here are the IPC-7351B standard spacing rules from the maximum component boundary to the minimum placement courtyard excess:

Least environment = 0.1 mm

Nominal environment = 0.25 mm

Most environment = 0.5 mm

There are different placement courtyard spacing rules for grid array packages based on ball size:

Ball size above 0.50 mm = 2 mm

Ball size between 0.50 mm & 0.25 mm = 1 mm

Ball size below 0.25 mm = 0.5 mm

One of the key aspects of the placement courtyard is that it allows room for rework. In the case of the BGAs, the larger the ball size, the larger the heat nozzles and removal equipment used for getting around and under the component to unsolder the contacts.

An important note to make here is that if you have no intentions of ever reworking (removing and replacing) a BGA component, the 2 mm placement courtyard is not necessary and a 0.5 mm courtyard excess is okay. This also is relevant to the "most environment" where the minimum courtyard excess is 0.5 mm on all SMT land patterns, i.e., the military and medical instrument industry might use the “most environment” and require "Class 3" *High Reliability Electronic Products* where continued high-performance is critical and product downtime cannot be tolerated. The Class 3 fabrication is very expensive and if a component on the PCB fails, rework becomes necessary to reduce cost. Rework requires additional land pattern placement courtyard excess to allow adequate space for rework equipment.

Alternatively, the "least environment" for high-density PCB layout, such as handheld devices, has a courtyard excess of 0.1 mm with no room for rework equipment. So, if a component fails in your cellular phone, it will not be sent back to the shop for rework, but instead, it will be discarded.

The placement courtyards can be placed next to each other so the outline overlaps; however, you need to discuss this with your assembly shop if they require an additional manufacturing zone for their process. The placement courtyard round-off snap grid is 0.5 mm. The question of "why don't you place the silkscreen outline outside the land pattern boundary" is a FAQ and this is the answer: "It is important that all silkscreen outline data be located inside the placement courtyard."

This rule includes the post-assembly inspection dot, which sometimes gets partially placed outside the placement courtyard. This is why, in the upcoming IPC-2614 for board fabrication documentation and drafting standards, the "post-assembly inspection ***dot***" will become the "post-assembly inspection ***line***" and it will look like this to keep them inside the placement courtyard outline. See Figure 3.

Also, the line in most cases has higher visibility on the assembled PCB. The post-assembly inspection marker is used for post-assembly QC for possible component inverted (incorrect) assembly orientation. The polarity marker on the component should align with the post assembly Inspection silkscreen marking.

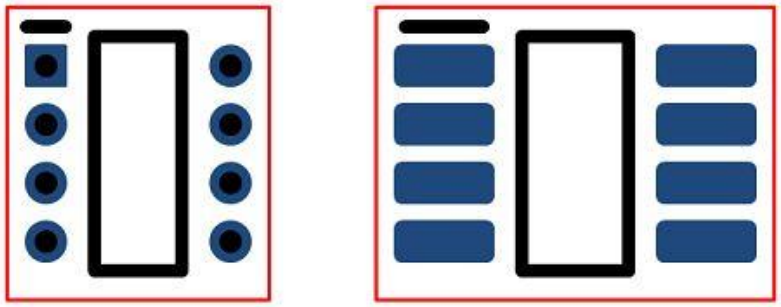


Figure 3. Post-assembly inspection lines inside placement courtyard.

The placement courtyard or courtyard excess is the smallest area that provides a minimum electrical and mechanical clearance of the maximum extremities of the land pattern and/or the component body. However, it is the responsibility of the user to verify the land patterns used for achieving an undisturbed mounting process including testing and an ensured reliability for the product stress conditions in use.

For many through-hole parts and connectors, the placement courtyard will follow the contour of the component body outline and land pattern. See Figure 4.

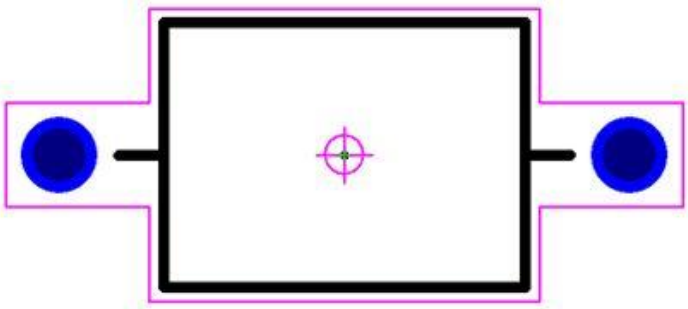


Figure 4. PTH resister courtyard.

Most enterprise CAD tools – for instance, Mentor Graphics Expedition Enterprise – have a different DRC checking feature that the user can define the component type to component type spacing rules. In this case, the placement courtyard excess should be turned off and the placement courtyard would be identical to the maximum component boundary. The maximum component boundary is a combination of whichever land pattern features, land (pad) or component body which protrude the most from the center.

Figure 5. Enterprise CAD tool placement courtyard.

The Enterprise CAD tool placement courtyard is not defined in the IPC-7351 standard. This concept is based on the Enterprise CAD tools ability to determine various components body to body spacing that are user-definable rules within the CAD tool options.

Land Calculation

IPC-7351B for SMT technology defines the rules for creating optimized land pattern CAD library parts using a three-tier system: Least (high density), Nominal (controlled environment) and Most (ruggedized and shock resistant). Many PCB designers and CAD librarians have heard about the IPC-7351B standard, but few people know how it works. The IPC LP Calculator has made life easy for the PCB design industry by automatically generating accurate land pattern data derived from component dimensions.

Land (Pad) Size and Location

These 7 factors are used to calculate the optimum land size:

Component Body Tolerance

Component Terminal Tolerance

Fabrication Tolerance

Placement Tolerance

Land Size Round-off

Land Spacing Round-off

Solder Joint Goals for Toe, Heel and Side

IPC-7351 identifies two component body dimensions: “A” (body width) and “B” (body length). The one SMT *Component Body Tolerance* that affects the land pattern is the minimum and maximum sizes of the component “lead span” (the dimension from lead tip to lead tip) dimension "L." This varies for different component packages. For gull wing or J-lead, it’s the distance from outside lead tip to tip. For chip resistors or capacitors, it’s the full tolerance of the overall body. The picture below represents the "L" dimension of a gull-wing lead component. See Figure 1.

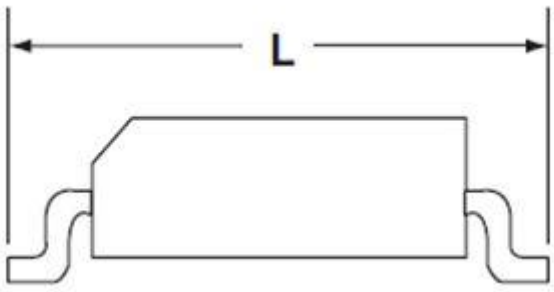


Figure 1. Lead span.

The ***Component Terminal Tolerance*** is the size of the metalized area that actually touches the land area. IPC refers to this as the component footprint. The footprint must compensate for the minimum and maximum lead tolerance for the calculation of an optimized land size. The component lead footprint is then synchronized with the appropriate land pattern. See Figure 2.

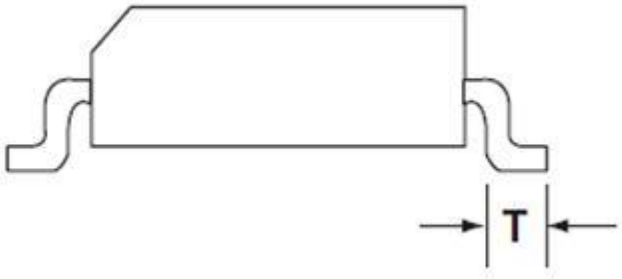


Figure 2. Terminal tolerance.

The ***Fabrication (Manufacturing) Tolerance*** compensates for the fabrication allowance for etchback. By adding a fabrication tolerance, we calculate the land area that we need after the fabrication etching process. The IPC-7351 fabrication tolerance is 0.05mm. See Figure 3.

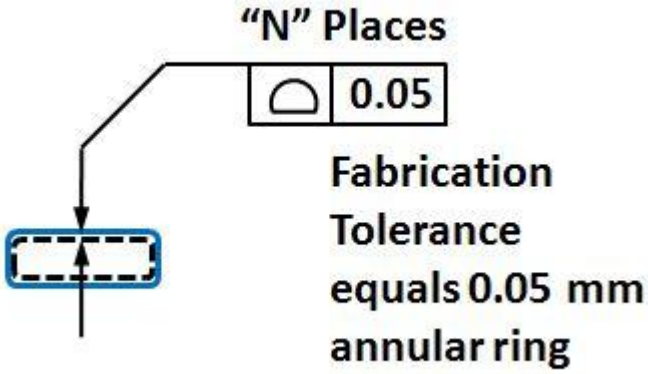


Figure 3. Fabrication tolerance.

The ***Placement (Assembly) Tolerance*** compensates for the pick-and-place machine accuracy. When parts are manually placed or machine placed, there is a small margin of placement accuracy that must be accounted for. The IPC-7351 assembly tolerance is 0.05mm.

Land Place (Spacing) Round-off relates to the land center to land center spacing. The goal in the IPC-7351 is to place all lands on a 0.05mm grid, so the space between the land span is rounded to 0.1mm increments so that the distance from the center of the land pattern to the center of the land is in 0.05mm increments. This plays a critical role in trace routing to achieve the highest packing density and cleanest routing results. In this example of a common chip component in Figure 4, the land snap grid is 0.05 mm from the center of the part to the center of the lands, the C1 and C2 dimensions.

Land Size Round-off is the value that the land size rounds up or down to. The IPC-7351 standards round land sizes to 0.05mm increments with the exception of micro-miniature component packages that are typically less than 1.6mm in size. The micro-miniature part land size round-off is set to 0.01mm increments. In Figure 4, the "X" & "Y" dimensions are rounded off in 0.05 mm increments. Even the land corner radius is rounded in 0.05 mm increments. When you export your PCB design layout database, all numbers for every design element should be in 0.05 mm increments. This greatly optimizes your PCB layout but also organizes all the graphics for best-in-class aesthetics for your PCB design layout.

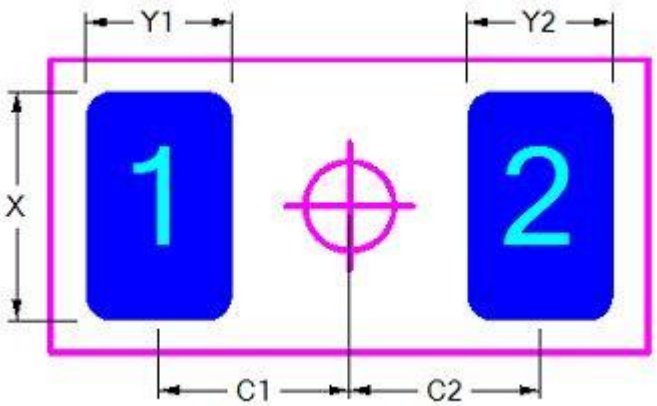


Figure 4. Land place and size round-off.

Solder Joint Goals for toe are usually the outside the component lead with two exceptions: With the J-lead and molded body components, the toe is under the component body. The heel goals are normally on the inside of the component lead and the side goals are for both sides of the component lead. In Part 5 of this series I listed the component lead forms. Every lead form has its unique solder joint goal table. Here is a sample table for the Least, Nominal and Most "Toe, Heel and Side" goals and the placement courtyard excess for the gull wing component family. Notice the round-off factor is in 0.05 mm increments. See Table 1.

Gull Wing Lead	Least Level C	Nominal Level B	Most Level A
Toe (J_T)	0.15	0.35	0.55
Heel (J_H)	0.25	0.35	0.45
Side (J_S)	0.01	0.03	0.05
Round-off factor	Round off to the nearest 0.05		
Courtyard excess	0.1	0.25	0.5

Table 1. Gull-wing solder joint goal table.

When all of the tolerances, round-offs and solder joint goals are applied the end result is a perfect land pattern. See Figure 5.

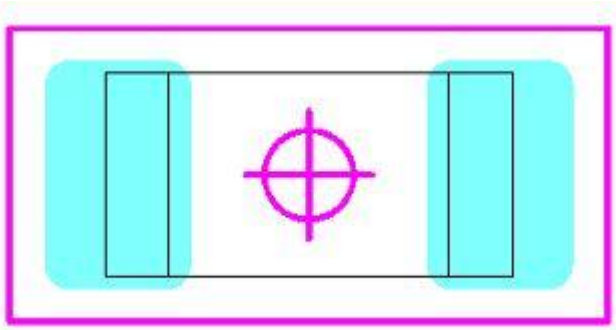


Figure 5. Land pattern and component with tolerances.

If all the tolerances and solder joint goals were removed from the mathematical model, the component lead would be equal to the land size. This is the starting point for all land size calculations. Figure 6 illustrates a chip component (black outline) without tolerances, round-offs, or solder joint goals and the land size (cyan) without a toe, heel or side goal.

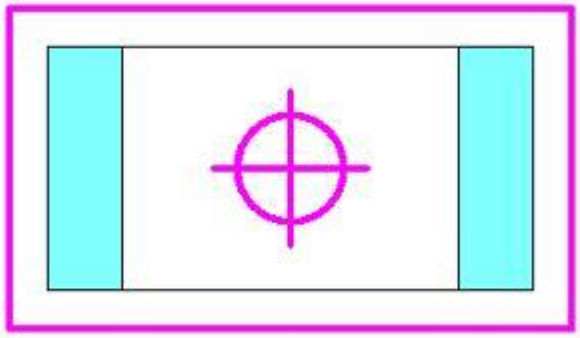


Figure 6. Land pattern and component.

The resulting solder joint for a chip component should look similar to this picture. Note that the component terminal never touches the land. There must be solder paste between the component lead and the land to form the best solder joint. See Figure 7. Here's a note from the IPC J-STD-001D "Requirements for Soldered Electrical and Electronic Assemblies." **Section 4.14 Solder Connection:** All solder connections **shall** indicate evidence of wetting and adherence where the solder blends to the solder surface.

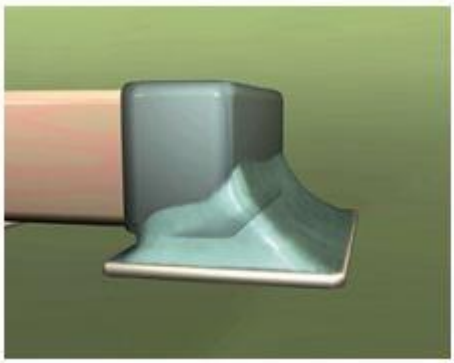


Figure 7. Chip solder joint.

Padstacks

Padstack creation is something every CAD tool will eventually have to incorporate because it expedites and optimizes the construction of CAD libraries. The SMT padstack is easy to define:

Top land

Top solder mask

Top paste mask

Top assembly

Last week, I explained land calculation for SMT land patterns, so let's discuss plated through-hole calculations in this segment.

The through-hole (PTH) padstack is complex. See Figure 1 of a through-hole padstack.

Drill hole

Top assembly

Top solder mask

Top land

Inner land

Plane thermal relief

Plane anti-pad (clearance)

Bottom land

Bottom solder mask

Bottom assembly

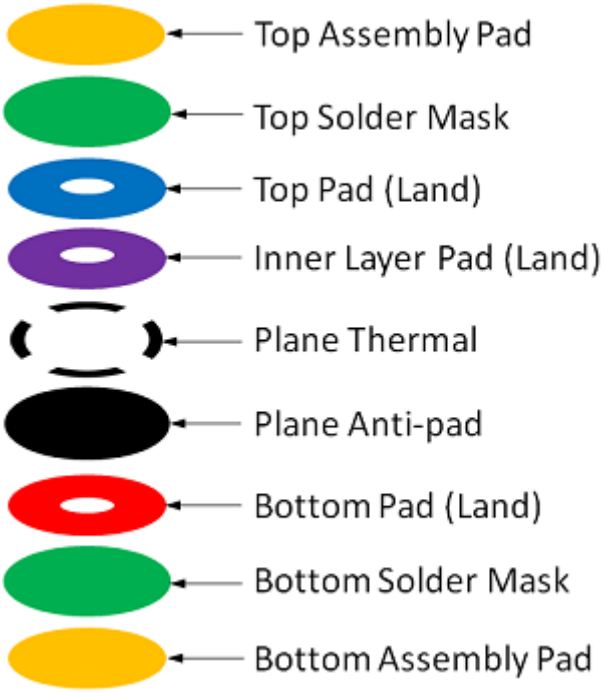


Figure 1. Plated through-hole padstack.

The PTH padstack creation can be fully automated via the maximum lead diameter. See Figure 2.

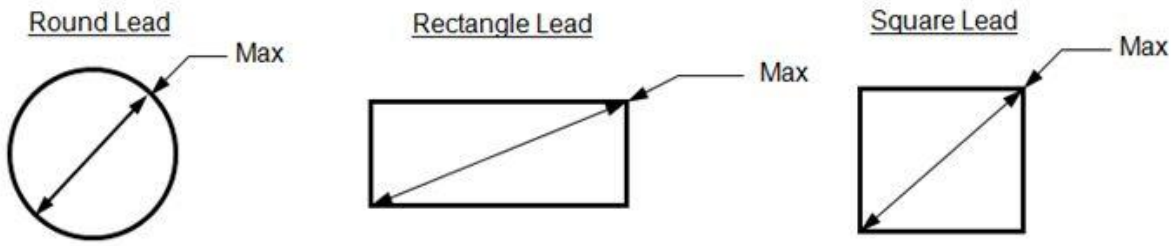


Figure 2. Plated through-hole maximum lead size.

IPC-2222 Table 9-3 has a hole size calculation chart for maximum lead + level = minimum hole size.

IPC-2222 Table 9-3		
Max Lead + Level = Min Hole		
Level A	Level B	Level C
0.25	0.2	0.15

IPC-2222, Table 9-3.

Once you calculate the hole size, add the minimum annular ring of 0.05 mm per IPC-2221 Table 9-2.

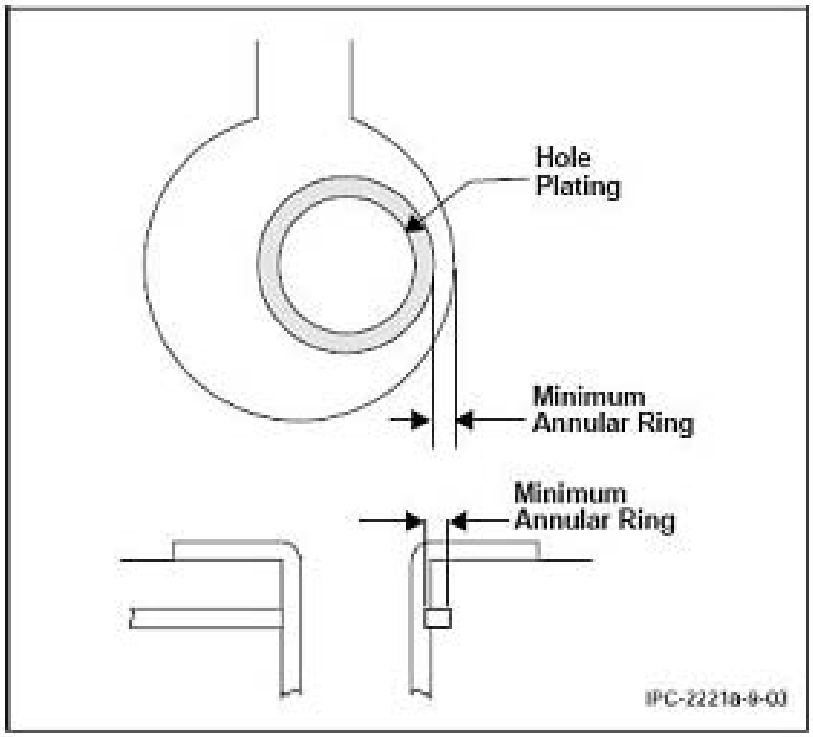


Figure 9-3 Internal Annular Ring

Table 9-2 Annular Rings (Minimum)

Annular Ring	Class 1, 2, and 3
Internal Supported	0.025 mm [0.00098 in]
External Supported	0.050 mm [0.00197 in]
External Unsupported	0.150 mm [0.005906 in]

Figure 3. IPC-2221 minimum annular ring.

Next we need to add the IPC-2221 Minimum Fabrication Allowance to the pad size in Table 9-1.

IPC-2221 Table 9-1		
Min Fabrication Allowance		
Level A	Level B	Level C
0.6	0.5	0.4

IPC-2221, Table 9-1.

So, the minimum annular ring X 2 + minimum fabrication allowance + maximum lead + hole over lead = pad diameter

Next we need to calculate the plane thermal relief ID, OD and spoke width sizes.

Thermal Spoke Width = 60%
Hole Dia divided by Spoke Qty
Round up to nearest 0.05 mm

Thermal ID over Hole Size		
Level A	Level B	Level C
0.6	0.4	0.3

Thermal OD over Hole Size		
Level A	Level B	Level C
1	0.7	0.5

Thermal OD over ID		
Level A	Level B	Level C
0.4 mm	0.25 mm	0.2 mm

Figure 4. Thermal relief calculations.

The plane anti-pad or plane clearance is the same size as the thermal relief OD (outside diameter).

In both the SMT and PTH padstack, the IPC-recommended solder mask and paste mask size is 1:1 scale of the top and bottom land size. The PCB fabrication shop can automatically oversize (swell) the solder mask to any size necessary to insure high yield production per their specific manufacturing capabilities. This is where automation of padstack generation comes in. The entire concept is to generate a padstack that meets the environment class of your design specification.

The IPC-7251 through-hole land patterns have the capability of accommodating all three performance classifications.

Producibility Levels

When appropriate, this standard will provide three design producibility levels of features, tolerances, measurements, assembly, testing of completion or verification of the manufacturing process that reflect progressive increases in sophistication of tooling, materials or processing and, therefore progressive increases in fabrication cost. These levels are:

Level A General Design Producibility – Preferred [Maximum land\lead to hole relationship]

Level B Moderate Design Producibility – Standard [Nominal land\lead to hole relationship]

Level C High Design Producibility – Reduced [Least land\lead to hole relationship]

Producibility levels are not to be interpreted as a design requirement, but a method of communicating the degree of difficulty of a feature between design and fabrication/assembly facilities. The use of one level for a specific feature does not mean that other features must be of the same level. Selection should always be based on the minimum need, while recognizing that the precision, performance, conductive pattern density, equipment, assembly and testing requirements determine the design producibility level. The numbers listed within the tables of IPC-7251 are to be used as a guide in determining what the level

of producibility will be for any feature. The specific requirement for any feature that must be controlled on the end item shall be specified on the master drawing of the printed board or the printed board assembly drawing.

Download the IPC-7251 padstack charts here - **AppNote 10835: IPC-7251 Padstack Charts**

Density Level A: Maximum Land/Lead to Hole Relationship – The 'maximum' land pattern conditions have been developed to accommodate the most robust producability of the solder application method. The geometry furnished may provide a wider process window for solder processing. The level A land patterns are usually associated with low component density product applications.

Density Level B: Nominal Land/Lead to Hole Relationship – Products with a moderate level of component density may consider adapting the 'median' land pattern geometry. The median land patterns furnished for all device families will provide a robust solder attachment condition for most soldering processes and should provide a condition suitable for wave, dip, drag or reflow soldering.

Density Level C: Least Land/Lead to Hole Relationship – High component density typical of portable and hand-held product applications may consider the 'minimum' land pattern geometry variation. Selection of the minimum land pattern geometry may not be suitable for all product use categories.

The "proportional" PTH padstacks are a mixture combination of all the IPC levels. Small holes use Level C and medium hole sizes use Level B and large hole sizes use Level A. When a hole size exceeds 2 mm, the proportional padstack annular ring will incrementally grow with every hole size. I have used the proportional padstacks for the past 20 years and it is proven technology that works. Its flexible flow is more compliant with the PTH components and their pin-pitch density. The main point is that proportional padstacks meet or exceed the IPC-7251 standard.

Note: the Producibility Levels are not necessarily related to the IPC Preformance Classifications, i.e., the IPC-7251 land patterns are capable of accommodating all three performance classifications.

IPC Performance Classifications

Three general end-product classes have been established to reflect progressive increases in sophistication, functional performance requirements and testing/inspection frequency. It should be recognized that there may be an overlap of equipment between classes.

The end product user has the responsibility for determining the ''use category'' or ''class'' to which the product belongs. The contract between user and supplier shall specify the class required and indicate any exceptions or additional requirements to the parameters, where appropriate.

Class 1 General Electronic Products – Includes consumer products, some computer and computer peripherals, and hardware suitable for applications where the major requirement is function of the completed assembly.

Class 2 Dedicated Service Electronic – Products Includes communications equipment, sophisticated business machines, and instruments where high performance and extended life is required, and for which uninterrupted service is desired but not mandatory. Typically the end-use environment would not cause failures.

Class 3 High-Reliability Electronic Products – Includes all equipment where continued performance or performance-on-demand is mandatory. Equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support systems and other critical systems.

Zero Component Orientation

A standard for component mechanical outlines and how they mount on a PCB is necessary to ensuring global commonality of design. In 2005 IPC and IEC (International Electrotechnical Commission) established a joint standard for land pattern geometries (IPC-7351/IEC 61188-5-1). To maintain a consistent method where these two important standards describe the component mechanical outlines and their respective mounting platforms, a single concept had to be developed that takes into account various factors within the global community.

The land pattern standards clearly define all the properties necessary for standardization and acceptability of a “One World CAD Library.” The main objective in defining this CAD library is to achieve the highest level of electronic product development automation. This encompasses all the processes involved from engineering to PCB layout to fabrication, assembly, and test. The data format standards need this type of consistency to meet the efficiency that electronic data transfer can bring to the industry.

Many large firms have spent millions of dollars creating and implementing their own unique internal standards for their own electronic product development automation. These internal standards are proprietary to each firm and are not openly shared with the rest of the industry. The result is a massive duplication of effort that costs the industry millions of man-hours in waste and creates industry chaos and global non-standardization.

The land pattern standards IPC-7351 and IEC 61188-5-1 put an end to the “proprietary intellectual property” and introduced a world standard so every electronics firm can benefit from electronic product development automation. The data format standards IPC-2581 and IEC 61182-2 are an open database XML software code that is neutral to all the various CAD ASCII formats. For true machine automation to exist, the world desperately needs a neutral CAD database format that all PCB manufacturing machines can read.

Fixed Component Orientation

One of the factors in global standardization is that of establishing a CAD component description and land pattern standard that adopts a fixed zero component orientation so that all CAD images are built with the same rotation for the purpose of assembly machine automation. IPC-7351 indicates that in the CAD library, all pin 1 locations are in the upper left corner for multiple pin components and pin 1 on the left for 2-pin components. Figure 1 represents IPC-7351 default and IEC 61188-7 Level A zero component orientation.

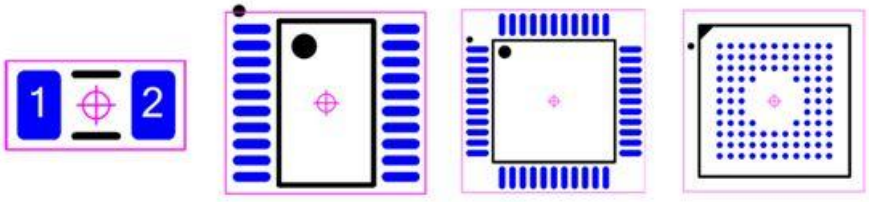


Figure 1. IPC-7351 zero component orientation with pin 1 in upper left corner.

In May 2009, the IEC land pattern committee voted and approved a new Level B Zero Component Orientation and redefined the IPC-7351 Zero Orientation as level A. The new IEC 61188-7 defines Zero Component Orientation pin 1 locations in the bottom left corner, except for 2-pin components where pin 1 is on the left side, and labeled it level B. Figure 2 represents IEC 61188-7 level B zero component orientation.

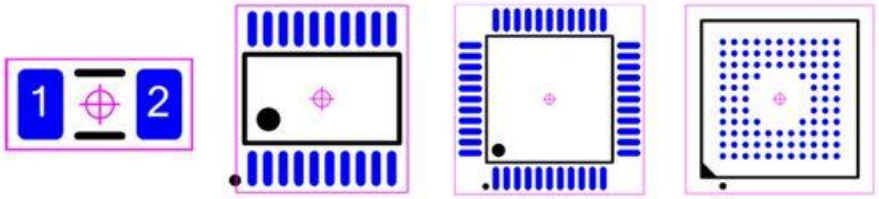


Figure 2. IEC 61188-7 zero component orientation with pin 1 in lower left corner.

Since the basic rules allow two variations of levels in the description of the CAD system library, it is a mandatory requirement to define which level was used (level A or level B) for the component descriptions in the data file. This information is a mandatory requirement in the header of any file that incorporates land patterns using these principles of zero-based orientation. See Figure 3 for the level A zero orientation and machine rotation.

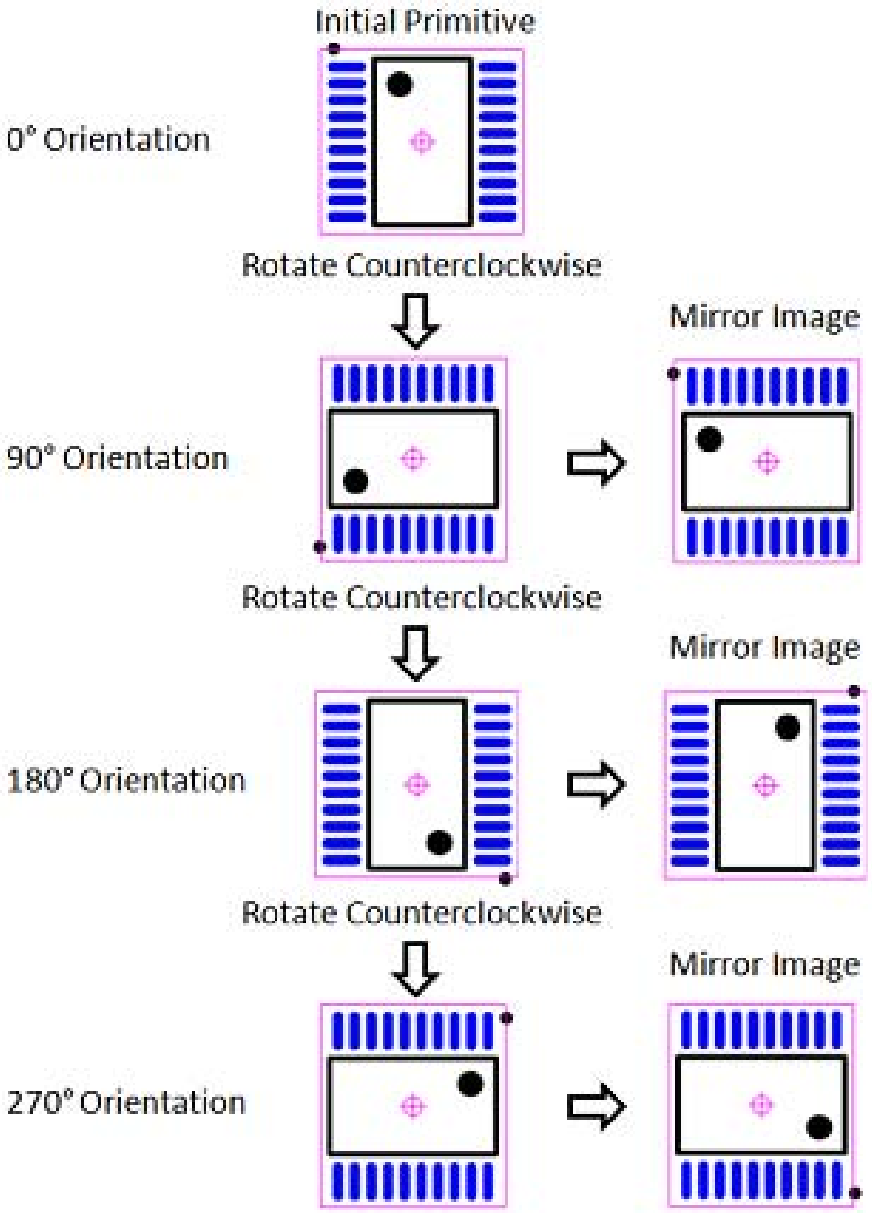


Figure 3. Example of “level A” orientation concepts.

The industry association Electronics Industry Association (EIA) is responsible for component descriptions and tape and reel orientation in the EIA-481-D standard. EIA has tried valiantly to influence the industry by making good standards that describe the component outlines and how they should be positioned in the delivery system to the equipment on the manufacturing floor. But parts suppliers have either not adhered to the recommendations or have misunderstood the intent and provided their products in different orientations.

Here are the EIA-481-D standard tape and reel illustrations (Figures 4 & 5) showing the quadrant designations.

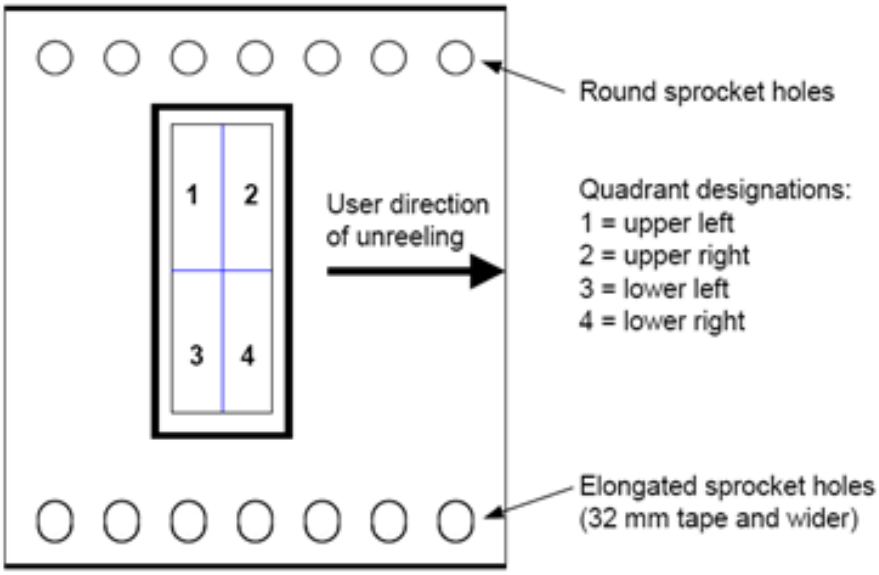


Figure 4. EIA-481-D quadrant designations.

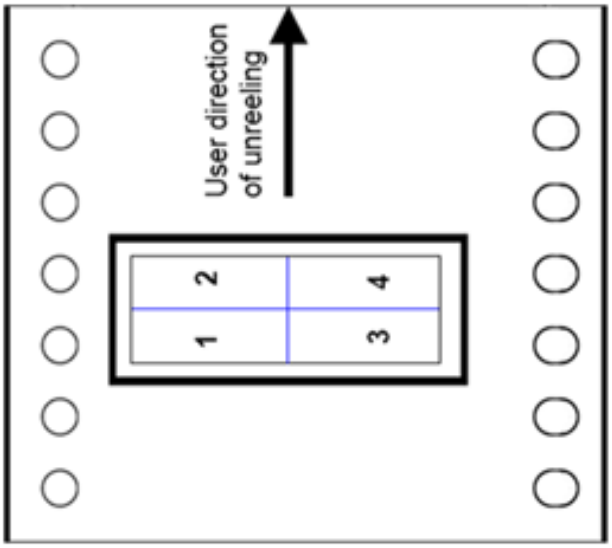


Figure 5. CAD library zero orientation quadrants.

IPC and IEC use consistent rotations throughout their standard where EIA uses multiple rotation variations

IPC-7x51 Level A uses Quadrant 2 for Pin 1 upper left, Quadrants 2-4 for upper center

IEC 61188-7 Level B uses Quadrant 1 for Pin 1 lower Left, Quadrants 1-2 for left center

EIA-481-D uses Quadrant 1 for Pin 1 lower left BGA, SOIC, SOP, QFN (rectangle), DIP

EIA-481-D uses Quadrant 2 for Pin 1 upper left TO-252, TO-263, QFN (square), TSOP

EIA-481-D uses Quadrant 3 for Pin 1 lower right for all SOT and miniature parts

EIA-481-D uses Quadrants 1-2 (Pin 1 left center) for PLCC, LCC

None of the 3 standards use Quadrant 4 for Pin 1 location

The main purpose of creating the land pattern standards is to achieve reliable solder joint formation platforms; the reason for developing the data transfer structure is to improve the efficiency with which engineering intelligence is converted to manufacturing reality. Even if the neutral CAD format can drive all the manufacturing machines, it would be meaningless unless the component description standard for CAD land patterns was implemented with some consistency. Zero component orientation has a key role in machine automation.

The easiest way to illustrate the three world standards is to list every component family and their respective zero component orientation for each standard. The big question: Which standard will prevail?

Component Family	IPC-7x51	IEC 61188-7	EIA-481-D
Chip (All Families)	Polarization On Left	Polarization On Left	Polarization On Left
Tantalum Capacitor	Polarization On Left	Polarization On Left	Polarization On Right
Molded Body Diode	Polarization On Left	Polarization On Left	Polarization On Left
SODFL	Polarization On Left	Polarization On Left	Polarization On Left
MELF	Polarization On Left	Polarization On Left	Polarization On Left
Aluminum Capacitor	Polarization On Left	Polarization On Left	Polarization On Left
Precision Inductors	Left	Left	Left
PLCC Square	Upper Center	Left Center	Left Center
PLCC Rectangle	Upper Center	Left Center	Left Center
LCC	Upper Center	Left Center	Left Center
QFP Square	Upper Left	Lower Left	Upper Left
QFP Rectangle	Upper Left	Lower Left	Lower Left
Bump QFP Side	Upper Left	Lower Left	Upper Left
Bump QFP Center	Upper Center	Left Center	Left Center
Ceramic QFP	Upper Left	Lower Left	Upper Left
SOIC	Upper Left	Lower Left	Lower Left
TSOP	Upper Left	Lower Left	Lower Left
TSSOP & SSOP	Upper Left	Lower Left	Upper Left
TSO8 (Mini US8)	Upper Left	Lower Left	Lower Right
BGA Square	Upper Left	Lower Left	Lower Left
BGA Rectangle	Upper Left	Lower Left	Lower Left
SOJ	Upper Left	Lower Left	Lower Left
CFP	Upper Left	Lower Left	Lower Left
QFN Square	Upper Left	Lower Left	Upper Left
QFN Rectangle	Upper Left	Lower Left	Lower Left
Chip Array	Upper Left	Lower Left	Lower Left
DFN	Upper Left	Lower Left	Lower Right
SON	Upper Left	Lower Left	Lower Right
SOT23-3	Upper Left	Lower Left	Lower Right
SOT23-5	Upper Left	Lower Left	Lower Right
SOT23-6	Upper Left	Lower Left	Lower Right
SOT89	Upper Left	Lower Left	Lower Right
SOT223	Upper Left	Lower Left	Lower Right
SOT143	Upper Left	Lower Left	Lower Right
SOTFL	Upper Left	Lower Left	Lower Right
SOT143 Reverse	Lower Left	Lower Left	Lower Left
TO-252	Upper Left	Lower Left	Upper Left
TO-263	Upper Left	Lower Left	Upper Left
LGA Square	Upper Left	Lower Left	Lower Left
LGA Rectangle	Upper Left	Lower Left	Lower Left
CGA Square	Upper Left	Lower Left	Lower Left
Oscillator (Multi-pin)	Upper Left	Lower Left	Lower Left
Crystal (2-pin)	Left	Left	Left
SMT Connectors	Left	Left	Left
PTH Connectors	Left	Left	Left
DIP	Upper Left	Lower Left	Lower Left
SIP	Left	Left	Left
Axial Lead	Polarization On Left	Polarization On Left	Polarization On Left
Radial Lead	Polarization On Left	Polarization On Left	Polarization On Left
PGA	Upper Left	Lower Left	Lower Left

You can download the complete IPC-7351B Electronic Component Zero Orientation document **here**.

0.5 mm Pitch BGA Routing Solution

Breakout and routing of large BGA packages with very fine pitch balls is a difficult task. But there is a reasonable solution for via fanout and a routing solution for the 0.5 mm pitch BGA – it just requires thinking outside the box.

Board thickness is an important factor because it affects the hole plating aspect ratio. If you use a 1 mm PCB thickness and want to achieve a 7:1 aspect ratio (common among all manufacturers), then the smallest hole size is 0.15 mm (6 mil). There are manufacturers who can hard drill a 0.15 mm (6 mil) hole through a 1 mm PCB. There are manufacturers who claim they can easily handle 10:1 aspect ratios. This means that they can drill 0.15 mm (6 mil) holes through 1.57 mm (0.062") thick PCB material and plate the hole without problems. Drilling all the way through the PCB is important because sequential lamination is an expensive process.

For all via-in-land technology, a thermal relief on the voltage and ground plane connections must be used to prevent cold solder joints. A direct via-in-land connection to the plane will dissipate the heat required to melt the solder around the BGA ball and this will result in a cold or cracked solder joint. The exception to this rule is if the via only contacts a single plane with ½ oz. copper or less.

If traces are routed between pins of the 0.5 pitch BGA land, the solder mask must be a 1:1 scale to create a "solder mask-defined" BGA land. In this way, the traces between the lands will be protected from exposure and possible short circuiting.

The 0.5 mm pitch BGA via-in-land drilled hole through the PCB is leading-edge technology. When laser drills are capable of producing 0.125 hole sizes all the way through the board and PCB manufacturers can accurately fill the holes with conductive metal epoxy, this technology will become mainstream.

Microvia technology is the mainstream solution for 0.5 pitch BGA components when a 0.1-0.15 laser hole is drilled one, two or three layers deep. This involves sequential lamination, but before we get to that subject, let's discuss the via fanout process. Using via-in-land technology, we must offset the drill holes to create adequate routing channels. This is the only routing solution that I know of to maintain manufacturability. See Figure 1 for a via fanout solution for the outer layer. Notice that you will have to add additional copper land for via annular ring.

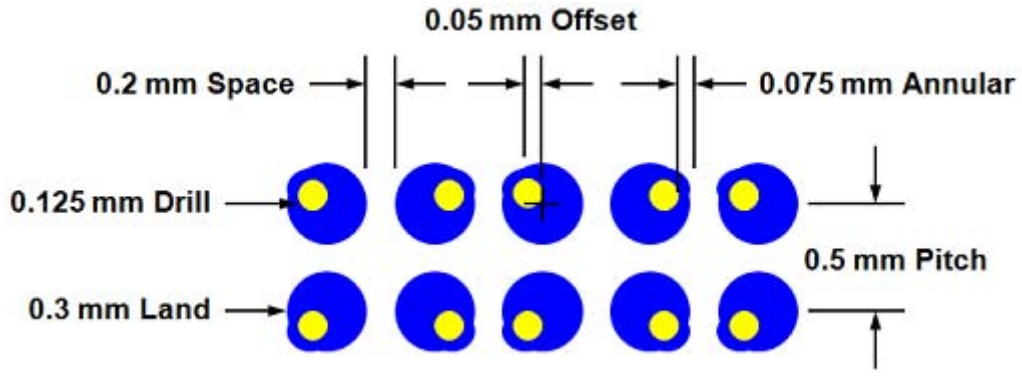


Figure 1. 0.5 mm pitch BGA offset via-in-land.

The vias are 0.05 mm offset from the land center and grouped together.

See Figure 2 for a via fanout solution for the inner layers. The most important feature here is the 0.1 mm (4 mil) trace width & 0.1 mm space between trace and via, and via and via.

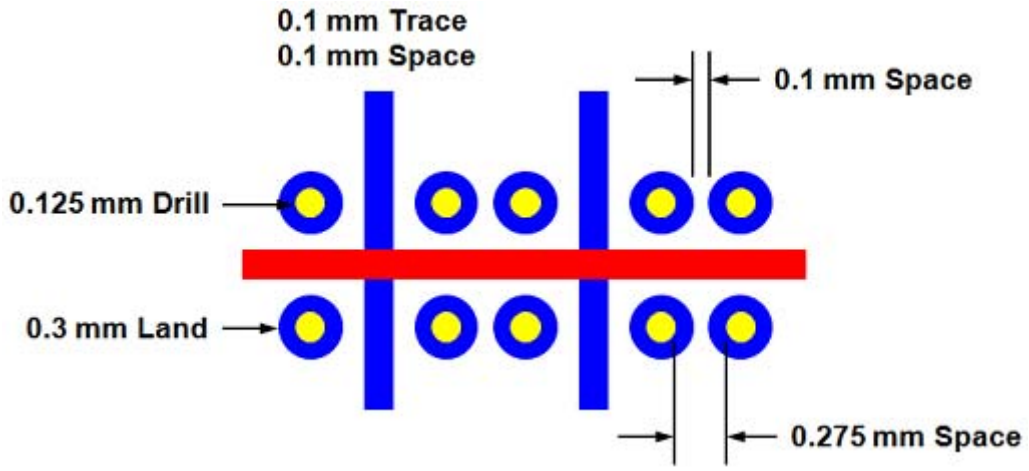


Figure 2. 0.5 mm pitch BGA fanout inner layers.

The number of rows and columns in the BGA will determine the number of routing layers required.

Sequential lamination process requires the inner layers to be laminated, drilled and plated in Phase 1, followed by the addition of two additional outer layers and back through lamination, drill and plate in Phase 2. Then add two additional outer layers and back through lamination, drill and plate in Phase 3.

See Figure 3 for the various phases of sequential lamination.

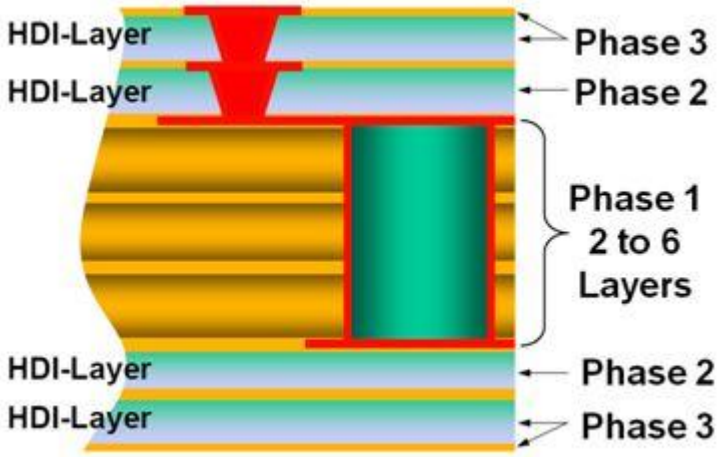


Figure 3. Phases of sequential lamination.

Let me try to explain why sequential lamination is so expensive and why most people avoid it unless they absolutely need it for high--volume production. The PCB inner layer manufacturing goes through the entire fabrication process in Phase 1. Then the first HDI layers that are added to the PCB have to go through the entire fabrication process over again. This basically doubles the cost in Phase 2. Then the second HDI layers that are added to the PCB have to go through the entire fabrication process over again. This basically triples the cost in Phase 3 and the manufacturers say that they are basically building the same PCB three times.

There are two methods of via drilling for sequential lamination: Staggered vias and stacked vias. See Figure 4 for the staggered microvia process.

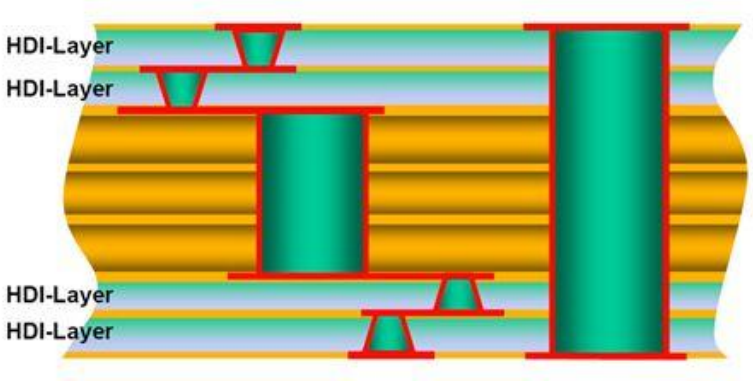


Figure 4. Staggered microvias.

Notice in the staggered microvia picture that the via plugging color is green. This could be an epoxy fill because the vias are staggered and there is no manufacturing stress. Discuss the benefits of staggered vs. stacked vias with your manufacturer to find out if one technique is less expensive than the other. See Figure 5 for the stacked microvia process.

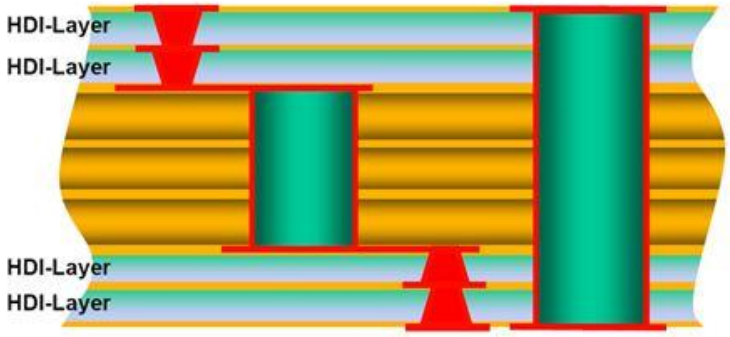


Figure 5. Stacked microvias.

The stacked microvias must be filled with conductive metal to prevent the outer laser drill from damaging the inner layer hole. See Figure 6.

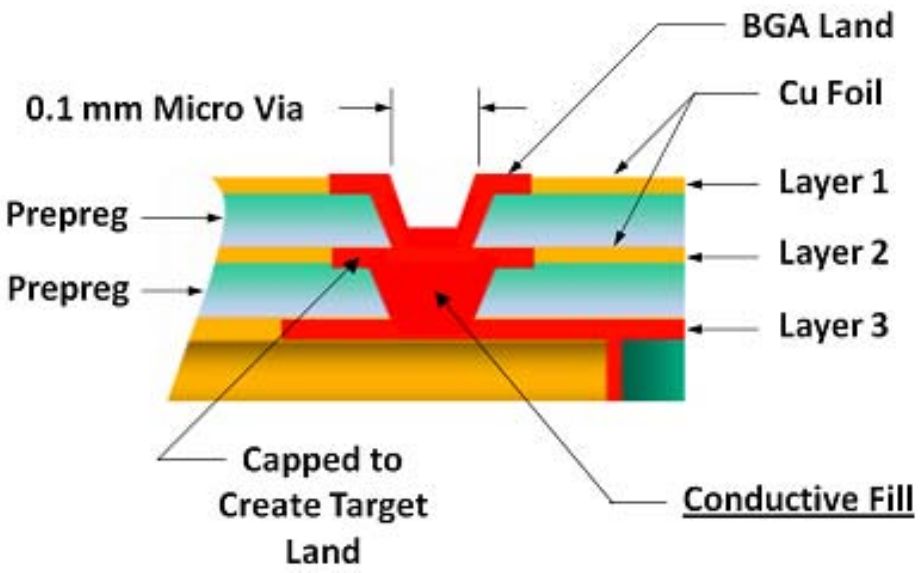


Figure 6. Stacked microvia conductive fill.

One example of the latest generation of via fill technology is MICROFILL EVF Copper Via Fill, by Dow Electronic Materials. See Figure 7 for stacked microvia conductive fill techniques.

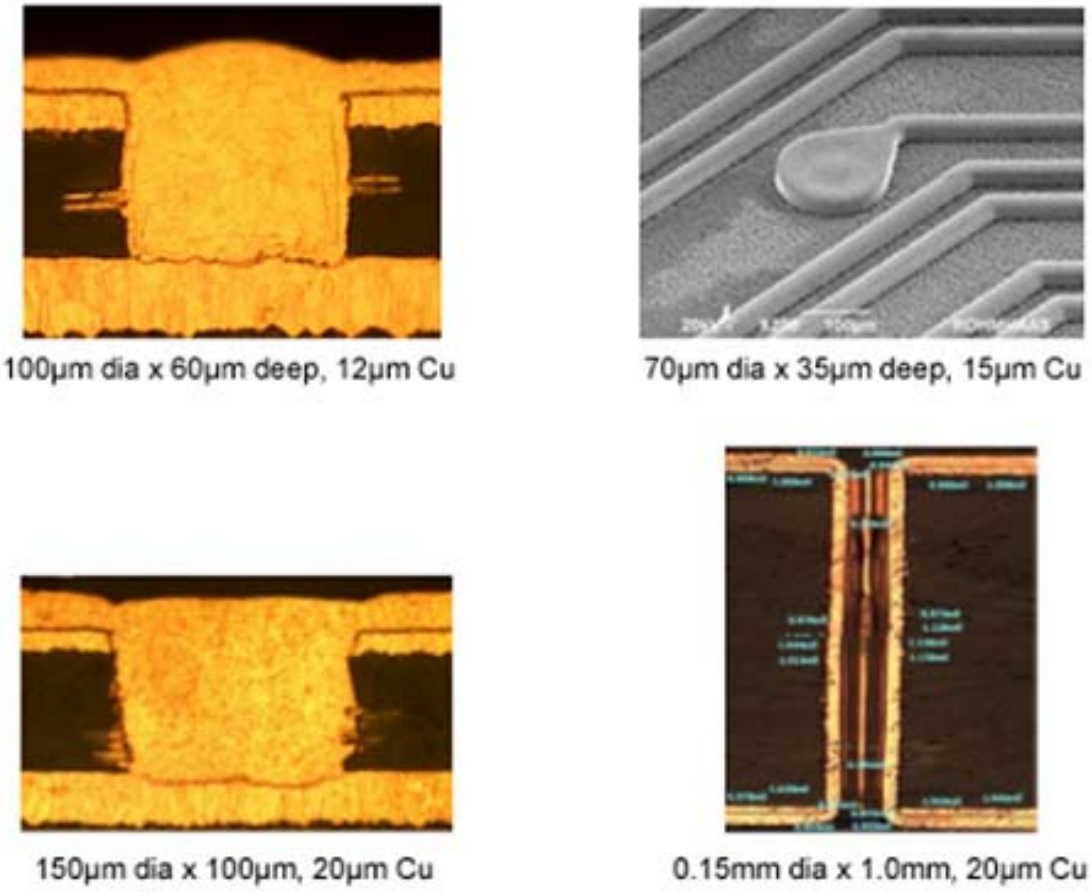


Figure 7. Stacked microvia conductive fill techniques.

Notice the lower right image in Figure 7 that shows a 0.15 mm via hole going all the way through a 1 mm thick PCB with 20um (0.000787”) or ½ oz. copper plating thickness. The normal hole plating thickness on an average PCB is 25um (0.001") or 1 mil.

The Three-Tier PCB Library

The three-tier PCB library concept was originally created by IEC (International Electromechanical Commission) in 1999 and introduced to IPC in 2000. The concept was created as a solution for high-density packaging for handheld devices, ruggedized military applications and everything in between.

The IPC-7351 and the IEC 61188-5-1 SMT land pattern standards were specifically created to introduce this new concept in 2005. Before 2005, the IPC-SM-782 was a one-tier land pattern standard developed in 1985 and released in March 1987. The pad size of the IPC-SM-782 land pattern, compared to the new IPC-7351, fell in between the “most” and the “nominal” environments.

The IPC-7251 land pattern standard for through-hole components is currently being developed. It also features a three-tier environment concept that applies to the hole sizes and annular rings.

Three land pattern geometry variations are supplied for each of the device families: Maximum Land Protrusion (Density Level A), Nominal Land Protrusion (Density Level B) and Least Land Protrusion (Density Level C). Here are the definitions for the three-tier (or 3 Level) PCB library system for both through-hole and SMD technology.

Density Level A: Maximum Land/Lead to Hole Relationship
The “maximum” land pattern conditions have been developed to accommodate the most robust produceability of the solder application method. The Level A land patterns are usually associated with low component density product applications. Level A land patterns accommodate wave or flow solder of leadless chip devices and leaded gull wing devices. The geometry furnished for these devices, as well as inward and “J-formed” lead contact device families, may provide a wider process window for reflow solder processes as well. Level A is used for ruggedized military applications and medical devices.

Density Level B: Nominal Land/Lead to Hole Relationship
Products with a moderate level of component density may consider adopting the “median” land pattern geometry. The median land patterns furnished for all device families will provide a robust solder attachment condition for most soldering processes and should provide a condition suitable for wave, dip, drag or reflow soldering. Level B is primarily used for desktop applications, controlled environment devices and many consumer electronic products.

Density Level C: Least Land/Lead to Hole Relationship
High component density typical of portable and handheld product applications may consider the “minimum” land pattern geometry variation. Selection of the minimum land pattern geometry may not be suitable for all product use categories.

The use of performance classes 1, 2, and 3 is combined with that of component density levels A, B, and C in explaining the condition of an electronic assembly. As an example, combining the description as Levels 1A, 3B or 2C would indicate the different combinations of performance and component density to aid in understanding the environment and the manufacturing requirements of a particular assembly.

See Figure 1 for an example of the three different land pattern levels for chip components.

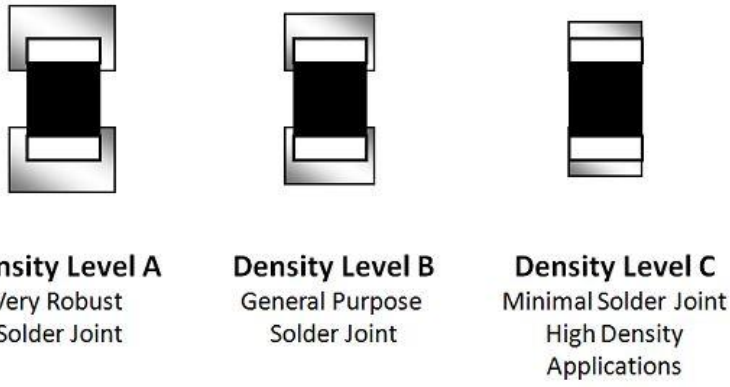


Figure 1. Three different land pattern levels.

Let's take a look at the IPC-7351B tables for the chip component family. Table 1 applies to all chip components equal to or larger than a 1608 (EIA 0603). The chip component family is referred to as "rectangular or square-end" components for resistors, capacitors and inductors.

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe	0.55	0.35	0.15
Heel	0.00	0.00	0.00
Side	0.05	0.00	-0.05
Round-off Factor	Round-off to the nearest 0.05 mm increment, i.e.: 1.00, 1.05, 1.10, 1.15		
Courtyard Excess	0.50	0.25	0.10

Table 1. IPC-7351B tables for chip components equal to or larger than the 1608 (EIA0603).

Notice in Table 1 that the side goal value for the "least environment" is -0.05 mm. This does not mean that the land will be smaller than the component lead. There are several other factors that go into the land size calculation like fabrication and assembly tolerances and component lead tolerance. So whenever you see a negative value in a solder joint goal table, it is only adjusting the land size to neutralize the fabrication tolerance.

Table 2 focuses on rectangular or square-end components for resistors, capacitors and inductors smaller than a 1608 (EIA 0603). Notice that the "toe" goal and placement courtyard excess are affected the most. Also, the round-off factor is in 0.02 mm increments.

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe	0.30	0.20	0.10
Heel	0.00	0.00	0.00
Side	0.05	0.00	-0.05
Round-off Factor	Round-off to the nearest 0.02 mm increment, i.e.: 1.00, 1.02, 1.04, 1.06		
Courtyard Excess	0.20	0.15	0.10

Table 2. IPC-7351B tables for chip components smaller than the 1608 (EIA0603).

See Figure 2 for an example of the three different land pattern levels for small outline package (SOP) components.

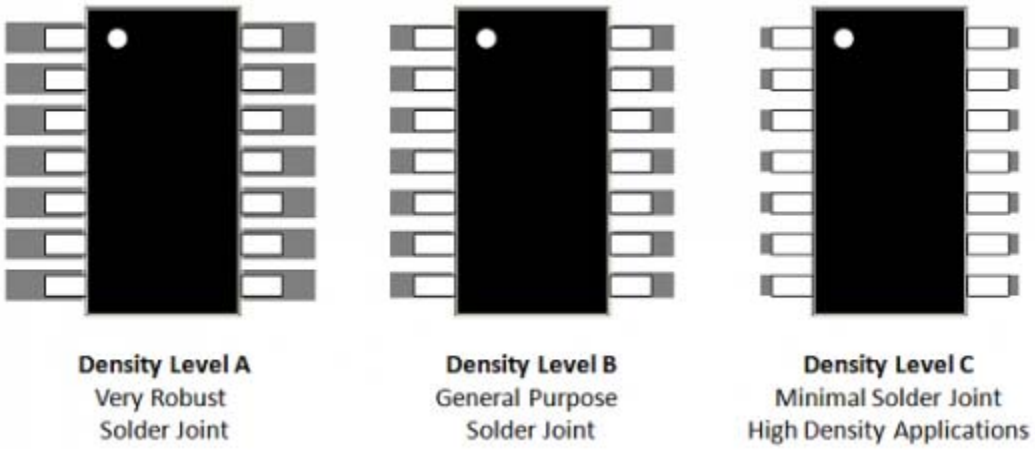


Figure 2. Three different land pattern levels for SOP components.

Let's take a look at the IPC-7351B tables for the gull-wing and flat ribbon L lead component family. This component family includes small outline diodes (SOD), small outline packages (SOP) small outline transistors (SOT) and quad flat packages (QFP). Table 3 applies to all gull-wing components with a pin pitch greater than 0.625 mm.

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe	0.55	0.35	0.15
Heel	0.45	0.35	0.25
Side	0.05	0.03	0.01
Round-off Factor	Round-off to the nearest 0.05 mm increment, i.e.: 1.00, 1.05, 1.10, 1.15		
Courtyard Excess	0.50	0.25	0.10

Table 3. IPC-7351B table for gull-wing components with a pin pitch greater than 0.625 mm.

Table 4 applies to the gull-wing and flat ribbon L lead component family with a pin pitch less than 0.625 mm.

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe	0.55	0.35	0.15
Heel	0.45	0.35	0.25
Side	0.01	-0.02	-0.04
Round-off Factor	Round-off to the nearest 0.05 mm increment, i.e.: 1.00, 1.05, 1.10, 1.15		
Courtyard Excess	0.50	0.25	0.10

Table 4. IPC-7351B table for gull-wing and flat ribbon L lead component family with a pin pitch less than 0.625 mm.

Notice in Table 4 that the only difference is in the "side" solder joint goal. Also, Table 4 only represents the small outline package (SOP) and the quad flat package (QFP) component families. There is a different IPC-7351B table for every component family lead type. The only component family group with just one tier for the land size is the grid array component family – the ball grid array (BGA), land grid array

(LGA), column grid array (CGA) and pillar column grid array (PCGA). This component family group has various placement courtyard excess sizes that are dependent on the lead size for the sole purpose of rework equipment access.

The “bottom only” leaded component families do not have a toe, heel or side solder joint goal. Their solder joint goal is referred to as a “periphery” and the land area is the same value on all sides. This includes D-shaped leads for pull-back lead QFN, square and rectangular leads for LGAs and round leads for BGA, CGA and LGA.

The SMT land pattern naming convention has an M, N or L at the end of the name; the PTH land pattern naming convention has an A, B or C at the end of the name to identify the density level with the exception of the grid array component families.

There is also a "proportional" environment for PTH libraries that uses a combination of IPC Level A, B and C depending on the hole size. Small holes use Level C, medium hole sizes use Level B, and larger hole sizes use Level C or greater annular ring.

Mounting Holes

Note: All numeric values in this article are in millimeters.

Mounting holes are found on every PCB design, but there is very little documentation about this topic. A Google or Wikipedia search on mounting holes renders no solutions for the PCB designer. Another issue that interferes with standardization is Imperial unit ANSI hardware and ISO metric hardware. So we're going to have to explain both unit systems for clarity. But first let's start with the basic fundamentals that both unit systems have in common.

Mounting hardware normally consists of the four items in Figure 1:

1.0 Phillips head screw
2.0 Hex nut
3.0 Flat washer
4.0 Lock washer

Figure 1. Typical mounting hardware.

There are four types of mounting holes:

1.0 Supported – Plated through with annular ring
2.0 Supported – Plated through with annular ring with vias
3.0 Unsupported – Non-plated and with copper pads
4.0 Unsupported – Non-plated and with no copper pads

The supported mounting hole is usually tied to the GND plane without a thermal relief (a direct connection is best) and the supported hole w/vias has both the main hole and the vias tied to the GND plane. Due to the fact that mounting hardware is never soldered to the PCB, there is no reason for a thermal relief pattern, and all holes (including vias) are connected directly to the plane. The unsupported (non-plated) holes have no connection to a GND plane layer and require defining an outer layer keep-out that compensates for hardware tolerances.

See Figure 2 for an illustration of the slop tolerance of a flat washer and the necessary copper keep-out sizing.

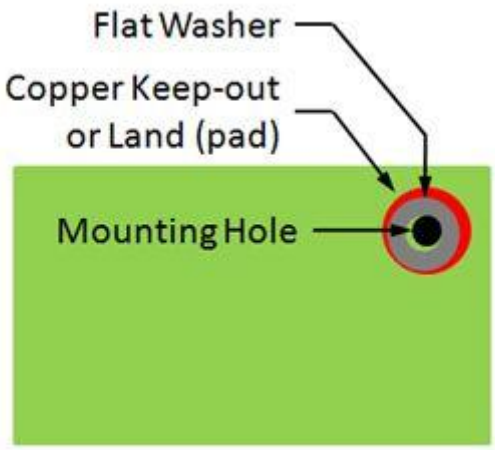


Figure 2. Slop tolerance of a flat washer and copper keep-out sizing.

There are two primary reasons for adding vias to the supported mounting hole. The first is to ensure that, if the screw threads stripped the copper plating from the main hole, the vias would still provide adequate ground connections. The second reason is for additional support to prevent the PCB from crushing if too much torque is used to tighten the nut. The average via hole size for mounting holes is 0.5 mm. See Figure 3 for a supported mounting hole with vias.

Figure 3. A supported mounting hole with vias.

See Table 1 for the most popular PCB hardware sizes for metric unit technology.

Metric Nut, Screw and Washer Hardware Sizes					
Screw Size Dia x Thread	Pan Head	Hex Nut	Flat Washer	Washer ID	Lock Washer
M2 x 0.4	4.00	4.62	5.30	2.20	4.40
M2.5 x 0.45	5.00	5.77	6.80	2.70	5.10
M3 x 0.5	6.00	6.35	7.30	3.20	6.20
M3.5 x 0.6	7.00	6.93	8.40	3.80	6.90

Table 1.

In Tables 2 and 4 there are three different padstack configurations for each metric screw size for land (pad) size calculations.

- No washer – pan head clearance
- Flat washer

The land (pad) diameter is equal to the hardware diameter and a placement courtyard is added to compensate for the slop tolerance indicated in Figure 2.

Note: These land (pad) and placement courtyard padstack values are in the “least” material values. You can add 0.25 mm for nominal or 0.5 mm for “most” land (pad) and placement courtyard environments. The hole sizes are for a loose fit.

ISO (metric) Hardware w/Plated Though Hole Padstack Data – Loose Fit									
Pan Head Screw Size	Hardware on PCB	Placement Courtyard	Hole Size	Top Pad	Inner Pad	Bottom Pad	Solder Mask	Plane Anti-Pad	Thermal Relief
M2 x 0.4	Pan Head	4.80	2.30	4.30	4.30	4.30	4.30	3.20	None
M2 x 0.4	Flat Washer	6.00	2.30	5.50	5.50	5.50	5.50	3.20	None
M2.5 x 0.45	Pan Head	5.90	2.85	5.40	5.40	5.40	5.40	3.70	None
M2.5 x 0.45	Flat Washer	7.60	2.85	7.10	7.10	7.10	7.10	3.70	None
M3 x 0.5	Pan Head	7.00	3.50	6.50	6.50	6.50	6.50	4.30	None
M3 x 0.5	Flat Washer	8.20	3.50	7.70	7.70	7.70	7.70	4.30	None
M3.5 x 0.6	Pan Head	7.90	3.90	7.40	7.40	7.40	7.40	4.80	None
M3.5 x 0.6	Flat Washer	9.20	3.90	8.70	8.70	8.70	8.70	4.80	None
ISO (metric) Hardware w/Non-Plated Though Hole Padstack Data – Loose Fit									
Pan Head Screw Size	Keep-out Size	Placement Courtyard	Hole Size	Top Pad	Inner Pad	Bottom Pad	Solder Mask	Plane Anti-Pad	Thermal Relief
M2 x 0.4	5.50	6.00	2.30	1.00	1.00	1.00	2.30	3.20	None
M2.5 x 0.45	7.10	7.60	2.85	1.00	1.00	1.00	2.90	3.70	None
M3 x 0.5	7.70	8.20	3.50	1.00	1.00	1.00	3.50	4.30	None
M3.5 x 0.6	8.70	9.20	3.90	1.00	1.00	1.00	3.90	4.80	None

Table 2.

See Table 3 for the most popular PCB hardware sizes for ANSI standards.

ISO (metric) Hardware w/Plated Though Hole Padstack Data – Tight Fit									
Pan Head Screw Size	Hardware on PCB	Placement Courtyard	Hole Size	Top Pad	Inner Pad	Bottom Pad	Solder Mask	Plane Anti-Pad	Thermal Relief
M2 x 0.4	Pan Head	4.60	2.10	4.10	4.10	4.10	4.10	3.20	None
M2 x 0.4	Flat Washer	5.80	2.10	5.30	5.30	5.30	5.30	3.20	None
M2.5 x 0.45	Pan Head	5.60	2.60	5.10	5.10	5.10	5.10	3.70	None
M2.5 x 0.45	Flat Washer	7.30	2.60	6.80	6.80	6.80	6.80	3.70	None
M3 x 0.5	Pan Head	6.60	3.10	6.10	6.10	6.10	6.10	4.30	None
M3 x 0.5	Flat Washer	7.80	3.10	7.30	7.30	7.30	7.30	4.30	None
M3.5 x 0.6	Pan Head	7.60	3.60	7.10	7.10	7.10	7.10	4.80	None
M3.5 x 0.6	Flat Washer	8.90	3.60	8.40	8.40	8.40	8.40	4.80	None
ISO (metric) Hardware w/Non-Plated Though Hole Padstack Data – Tight Fit									
Pan Head Screw Size	Keep-out Size	Placement Courtyard	Hole Size	Top Pad	Inner Pad	Bottom Pad	Solder Mask	Plane Anti-Pad	Thermal Relief
M2 x 0.4	5.30	5.80	2.10	1.00	1.00	1.00	2.10	3.20	None
M2.5 x 0.45	6.80	7.30	2.60	1.00	1.00	1.00	2.60	3.70	None
M3 x 0.5	7.30	7.80	3.10	1.00	1.00	1.00	3.10	4.30	None
M3.5 x 0.6	8.40	8.90	3.60	1.00	1.00	1.00	3.60	4.80	None

Table 3.

ANSI Nut, Screw and Washer Hardware Chart					
Screw Size	Pan Head	Hex Nut	Flat Washer	Washer ID	Lock Washer
#2-48	4.24	5.51	6.35	2.39	4.36
#4-40	5.56	7.34	9.52	3.18	5.31
#6-32	6.85	9.17	11.13	3.96	6.35
#8-32	8.18	10.08	12.70	4.78	7.44

Table 4.

ANSI Hardware w/Plated Though Hole Padstack Data – Loose Fit									
Pan Head Screw Size	Hardware on PCB	Placement Courtyard	Hole Size	Top Pad	Inner Pad	Bottom Pad	Solder Mask	Plane Anti-Pad	Thermal Relief
#2 - 48	Pan Head	5.00	2.45	4.50	4.50	4.50	4.50	3.40	None
#2 - 48	Flat Washer	7.40	2.45	6.90	6.90	6.90	6.90	3.40	None
#4 - 40	Pan Head	6.60	3.70	6.10	6.10	6.10	6.10	4.50	None
#4 - 40	Flat Washer	10.60	3.70	10.10	10.10	10.10	10.10	4.50	None
#6 - 32	Pan Head	7.80	3.90	7.30	7.30	7.30	7.30	4.80	None
#6 - 32	Flat Washer	12.50	3.90	12.00	12.00	12.00	12.00	4.80	None
#8 - 32	Pan Head	9.10	4.60	8.60	8.60	8.60	8.60	5.60	None
#8 - 32	Flat Washer	14.30	4.60	13.80	13.80	13.80	13.80	5.60	None
ANSI Hardware w/Non-Plated Though Hole Padstack Data – Loose Fit									
Pan Head Screw Size	Keep-out Size	Placement Courtyard	Hole Size	Top Pad	Inner Pad	Bottom Pad	Solder Mask	Plane Anti-Pad	Thermal Relief
#2 - 48	5.50	7.40	2.45	1.00	1.00	1.00	2.45	3.40	None
#4 - 40	7.10	10.60	3.70	1.00	1.00	1.00	3.70	4.50	None
#6 - 32	9.00	12.50	3.90	1.00	1.00	1.00	3.90	4.80	None
#8 - 32	10.85	14.30	4.60	1.00	1.00	1.00	4.60	5.60	None

Table 5.

ANSI Hardware w/Plated Though Hole Padstack Data – Tight Fit									
Pan Head Screw Size	Hardware on PCB	Placement Courtyard	Hole Size	Top Pad	Inner Pad	Bottom Pad	Solder Mask	Plane Anti-Pad	Thermal Relief
#2 - 48	Pan Head	4.80	2.25	4.30	4.30	4.30	4.30	3.40	None
#2 - 48	Flat Washer	7.20	2.25	6.70	6.70	6.70	6.70	3.40	None
#4 - 40	Pan Head	6.20	3.30	5.70	5.70	5.70	5.70	4.50	None
#4 - 40	Flat Washer	10.20	3.30	9.70	9.70	9.70	9.70	4.50	None
#6 - 32	Pan Head	7.50	3.60	7.00	7.00	7.00	7.00	4.80	None
#6 - 32	Flat Washer	12.20	3.60	11.70	11.70	11.70	11.70	4.80	None
#8 - 32	Pan Head	8.90	4.30	8.40	8.40	8.40	8.40	5.60	None
#8 - 32	Flat Washer	14.00	4.30	13.50	13.50	13.50	13.50	5.60	None
ANSI Hardware w/Non-Plated Though Hole Padstack Data – Tight Fit									
Pan Head Screw Size	Keep-out Size	Placement Courtyard	Hole Size	Top Pad	Inner Pad	Bottom Pad	Solder Mask	Plane Anti-Pad	Thermal Relief
#2 - 48	6.70	7.20	2.25	1.00	1.00	1.00	2.25	3.40	None
#4 - 40	9.70	10.20	3.30	1.00	1.00	1.00	3.30	4.50	None
#6 - 32	11.70	12.20	3.60	1.00	1.00	1.00	3.60	4.80	None
#8 - 32	13.50	14.00	4.30	1.00	1.00	1.00	4.30	5.60	None

Table 6.

The “loose fit” mounting holes are normally used on large boards greater than 100 mm (4”) and the “tight fit” mounting holes are commonly used for smaller board sizes.

There are some differences in hardware manufacturer’s feature sizes, so make sure that the hardware you use is adequately covered with the correct pad size and/or keep-out.

There are three tiers for the mounting hole family, but the only difference is the “placement courtyard excess.”

- Least – 0.1 mm annular
- Nominal – 0.25 mm annular
- Most – 0.5 mm annular

The QFN Family

The quad flat no-lead (QFN) component family, as seen in Figure 1, is one of the newest electronic packages to be introduced into PCB design. The QFN has pins on 4 edges of the bottom surface of the package. The QFN can have either a square or rectangle body as well as symmetric or asymmetric terminal patterns. The QFN with symmetric pins is only available in millimeter pin pitches of 0.8 mm, 0.65 mm, 0.5 mm and 0.4 mm as per the standard JEDEC MO-220I.

The QFN was introduced to replace the gull-wing lead Quad Flat Package (QFP) because the component leads are embedded in the plastic and cannot be bent during handling to insure consistent assembly attachment. The embedded lead form is also compatible with high-speed design as the die-to-lead bonding and PCB contact is much shorter. Plus, due to the high-speed aspect, the component generates a lot of heat. This is why most QFN packages have a thermal tab that is via stitched to the GND planes for heat dissipation.

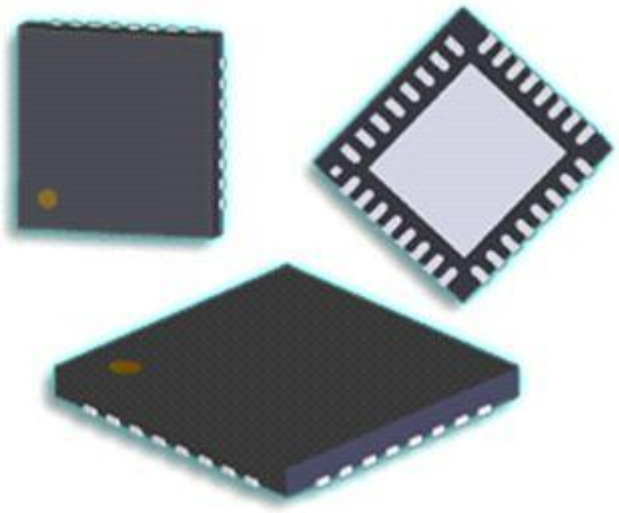


Figure 1. QFN packages.

The QFN package is a CSP (plastic encapsulated package) with a copper lead frame substrate. The package is leadless where electrical contact to the PCB is made by soldering the leads on the bottom surface of the package to the PCB, instead of the conventional formed perimeter gull wing leads. The design of the QFN package has enhanced electrical performance that enables the standard 2 GHz frequency to be increased up to 10 GHz with some design considerations.

The QFN leads are coated with a finish that provides environmental protection and maintains solderability. See Figure 2 for a cross-section internal view of the QFN package construction.

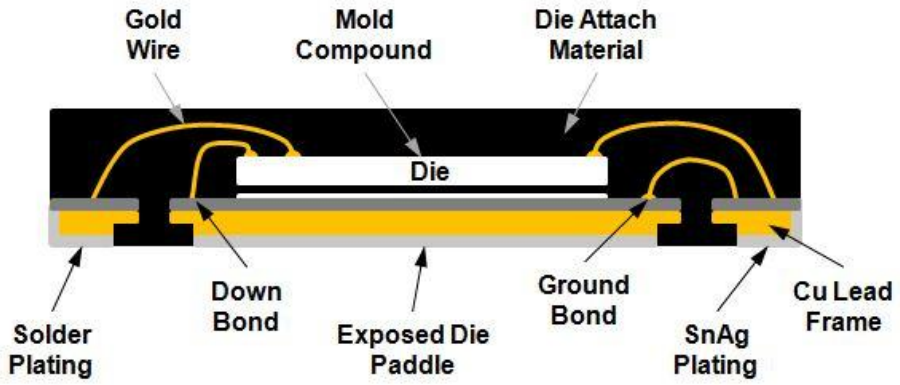


Figure 2. Cross-section of the QFN package.

The symmetric termination leads can be either rounded ends or rectangle ends. See Figure 3 for the 2 different lead styles.

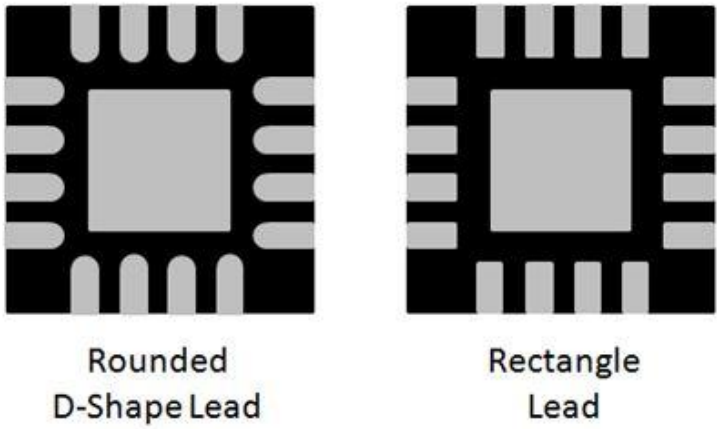


Figure 3. The symmetric QFN can use either rounded or rectangle leads.

The QFN uses the “flat no-lead edge” component lead style. See Figure 4 for a side view of the component lead. The component lead terminals are embedded in the plastic body and sticks out 0.05 mm on the bottom and wraps up the component body side by 0.2 mm.

Figure 4. Side view of the QFN.

There are 2 types of QFN component package styles: Standard and Flanged. The Standard package is commonly known as the “saw cut” package and the Flanged type is known as “molded body.” See Figure 5 for the 2 types of component package styles.

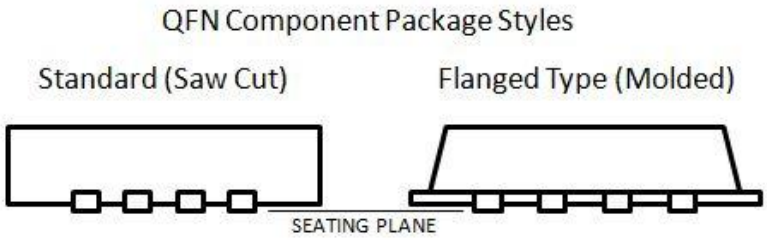


Figure 5. The two types of package styles are standard (L) and flanged (R).

The three-tier solder joint goals for the QFN component family have a toe, heel and side fillet. See Table 1 for the QFN solder joint goal data.

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe	0.40	0.30	0.20
Heel	0.00	0.00	0.00
Side	-0.04	-0.04	-0.04
Round-off Factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard Excess	0.5	0.25	0.1
Note: The rational for the “0.00 heel goal” and “-0.04 side goals” is that the land size is compensated from the lead tolerance and fabrication and assembly tolerances.			

Table 1.

The thermal tab shape can have a chamfered corner closest to the location of Pin 1. The “land size” is identical to the maximum tolerance of the thermal tab size. The solder mask size is 1:1 scale of the land size. The thermal tab can also have corner radius on the other corners. See Figure 6 for an example of a thermal tab with chamfered and rounded corners.

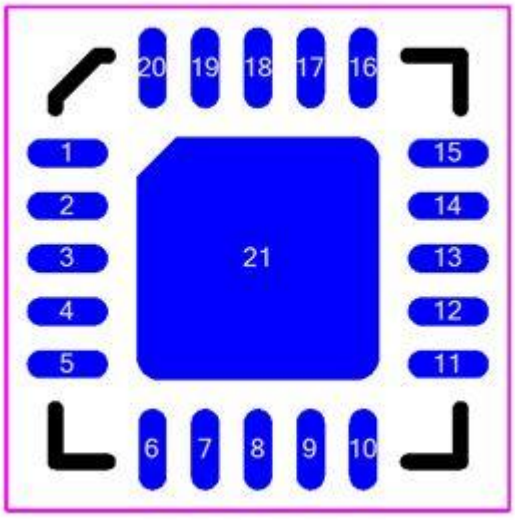


Figure 6. Thermal tab example.

The thermal pad paste mask size needs to be between 40% and 60% of the land size and is broken up into a checkerboard pattern. The IPC LP Calculator is set to 40% paste mask reduction by default, but the reduction percentage is user definable. The checkerboard pattern does not start until the thermal pad size exceeds 4.5 mm because the minimum paste mask aperture opening for thermal pad paste mask is about 1 mm square.

See Figure 7 for examples of thermal tab paste mask with a 40% reduction. The picture of the left has a thermal pad size of 4 mm and a single paste mask of 2.5 mm. The picture on the right has a thermal pad size of 4.5 mm and a matrix of 4 squares of paste mask of 1.4 mm.

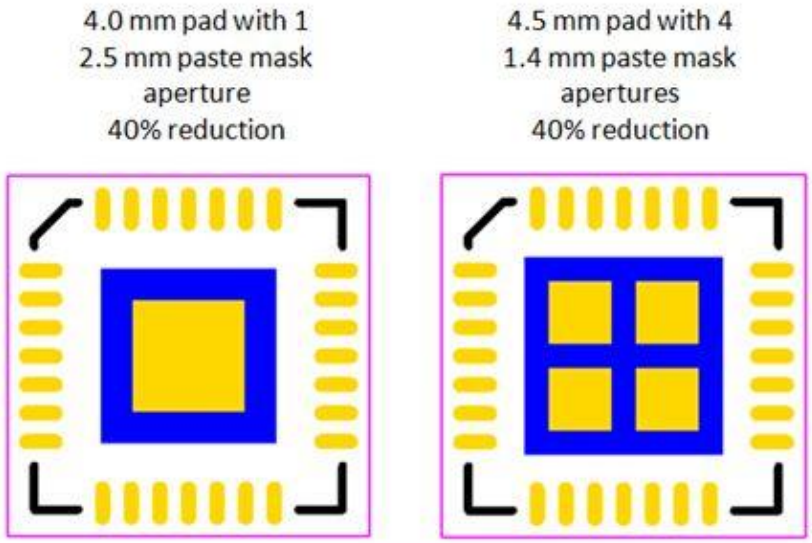


Figure 7. Thermal tab paste mask with 40% reduction; 4mm (L) and 2.5mm (R).

If there was no reduction of paste mask, the physical component would float on top of 0.15 mm (the thickness of the paste mask stencil) of solder. During the reflow process users have observed that the liquidus solder lifts the device and creates a pivot point near the center of the die attach pad (DAP). As the solder cools the device tends to tilt toward one side, often creating shorts in one area and opens in another. By reducing the paste mask stencil to 40% of the land size, the component will settle down evenly to allow for an adequate solder joints on the end termination leads. See Figure 8 for an example of excessive solder and reduced solder on the die attach pad.

Figure 8. Without paste reduction, solder can lift the device as shown on the left.

The primary purpose of the thermal tab is to conduct heat away from the die during operation. The best way to achieve this goal is to add stitch vias attached to the GND plane. The via hole size recommendation is 0.25 mm and should be plated, plugged and surface finished to prevent liquidus solder from entering the holes. By no means attempt to tent the vias with dry film solder mask because this will reduce the solder volume area on the pad. The via padstack is 0.5 mm pad, 0.7 mm plane clearance, 0.25 mm hole and no thermal relief. Placing the vias on a 1 mm grid allows for two 0.1 mm trace/space routing technology on all inner layers and opposite side. See Figure 9 for an example of a via matrix in a thermal pad.

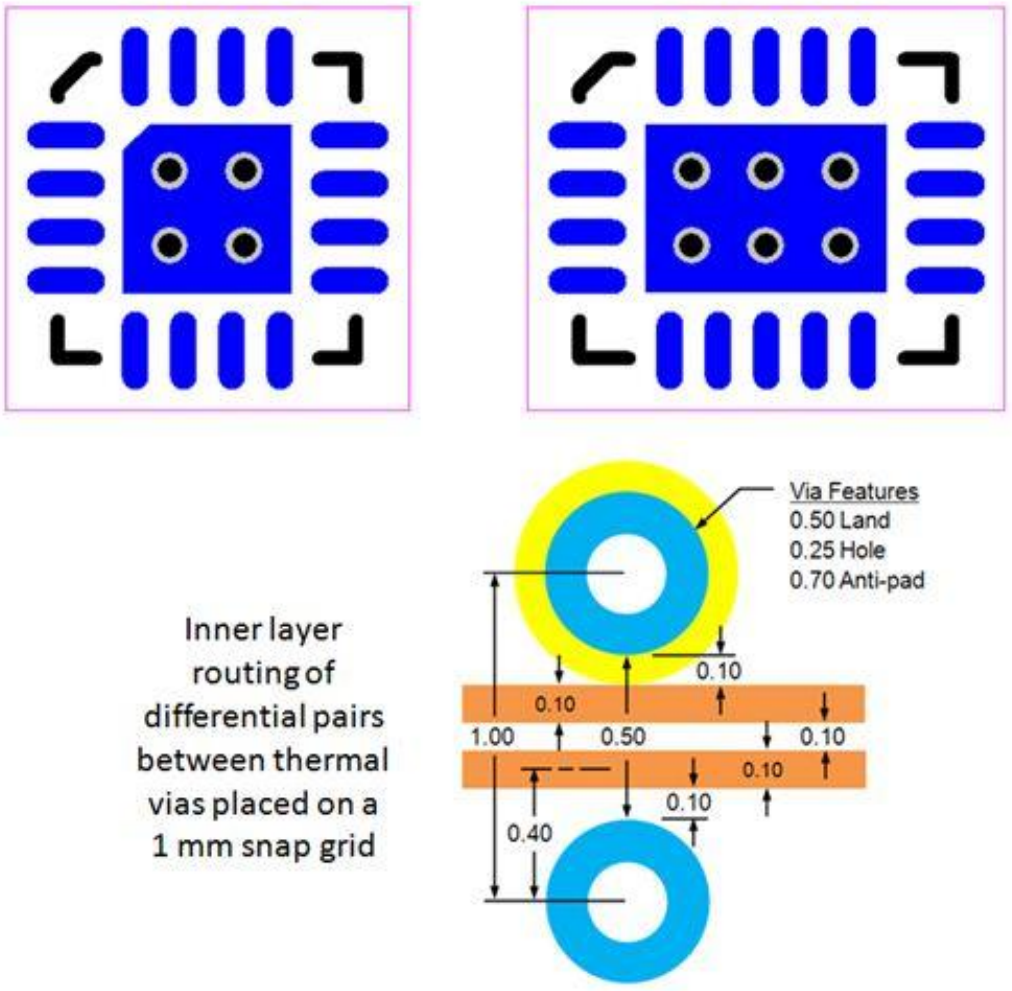


Figure 9. Via matrix example for thermal pad connection.

Some QFN packages come in a variety of lead sizes and multiple thermal tabs. See Figures 10 – 12 for some unique QFN variations.

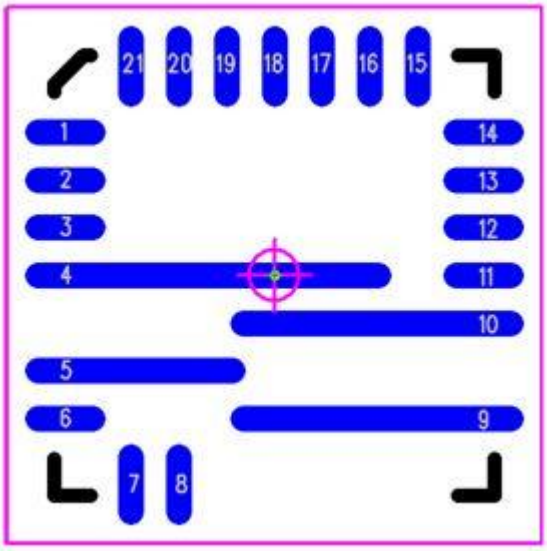


Figure 10. Multiple lead lengths, deleted pins and no thermal tab.

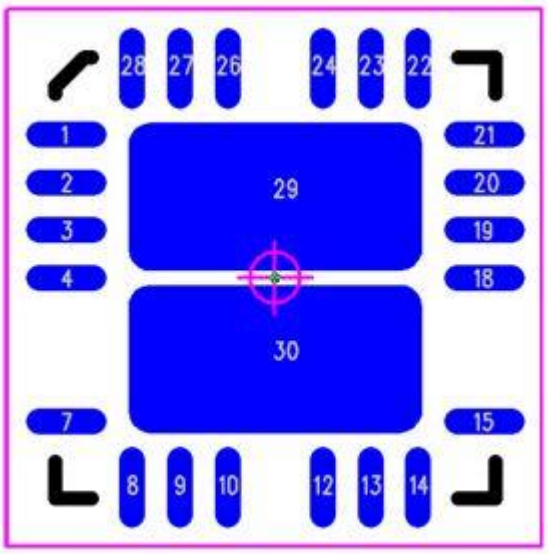


Figure 11. Multiple thermal tabs and “hidden pins.”

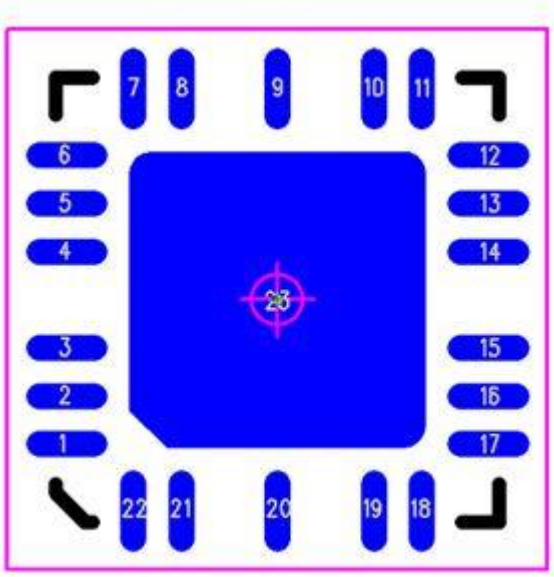


Figure 12. QFN has deleted pins and Pin 1 is lower left corner and pin order is counterclockwise.

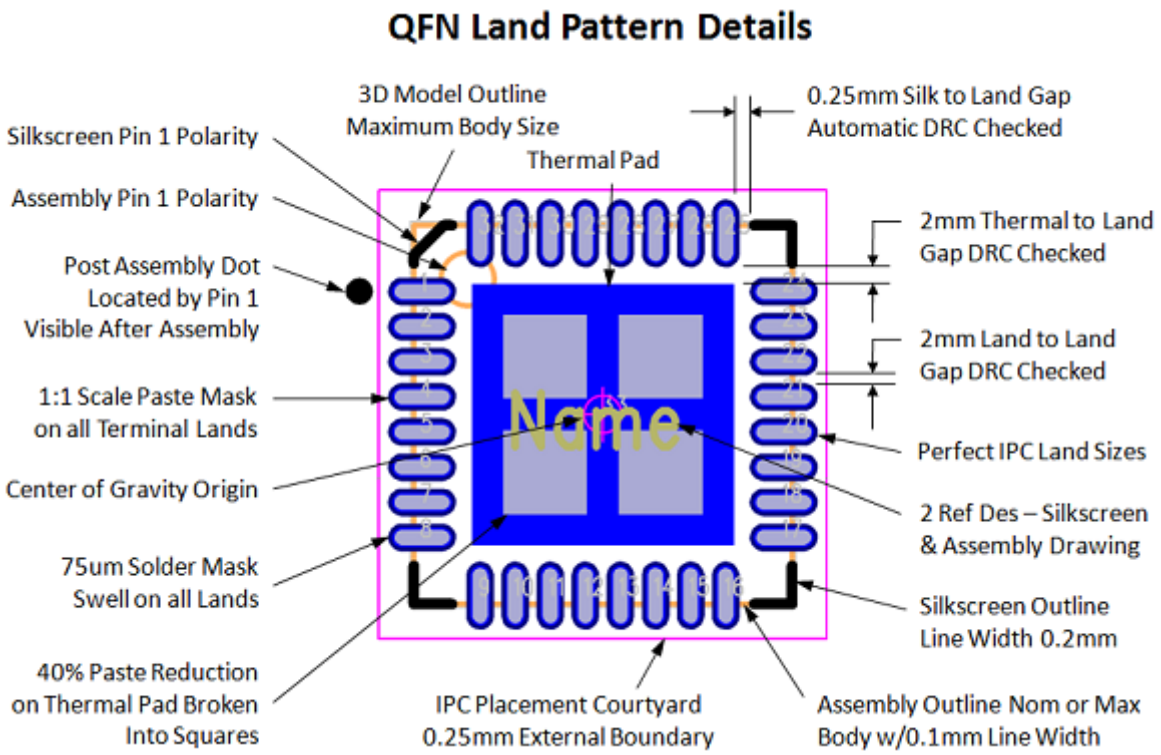


Figure 13. Picture of all the aspects that go into the construction of a QFN land pattern library part.

The via fanout for the QFN component family is really easy for all pin pitches that are on even 0.1 mm increments. These are 0.8 mm, 0.5 mm and 0.4 mm pin pitch. All SMT components with a 0.65 mm pin

pitch are not 100% compatible with the 0.05 mm universal grid system. It would be superior if the component manufacturer's never created any pin pitch in 0.05 mm increments. It would be much better for the PCB designer if all pin pitches were in 0.1 mm increments. In this case, 0.65 mm pin pitch would be superior if it was 0.6 mm.

Let's take a look at some of the via fanout solutions to optimize routing channels. These are shown in Figures 14 through 17. All of the routing solutions use the identical via size (0.5 mm pad, 0.7 mm anti-pad and 0.25 mm hole) and trace/space (0.1 mm) technology that is located in Figure 9.

Shown in Figure 14 is a 0.8 mm QFN sample via fanout and routing channel solution. This routing solution provides for 1 trace between vias. The red traces are the opposite side and the green traces are the inner layer. The yellow annular ring on the via is the plane clearance.

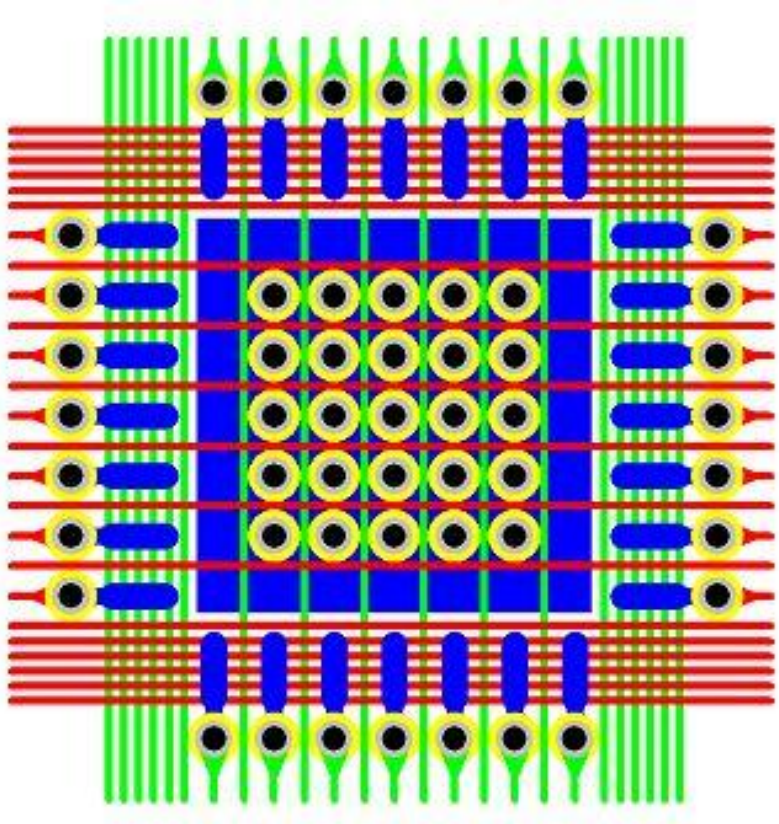


Figure 14. Sample fanout for 0.8mm QFN.

Figure 15 is a 0.65 mm QFN via fanout and routing channel solution. The 0.65 mm pitch fanout must use a 0.05 mm grid and 3 traces between vias. When there is an even number of pins on each side, you have to use a 0.025 mm grid system because the components are always placed on a 0.1 mm grid system and from the center of the 0.65 mm QFN to the center of the pad is 0.65, which divided by 2 = 0.325 mm. This is why 0.65 mm pitch components are not optimized for the universal 0.05mm grid system.

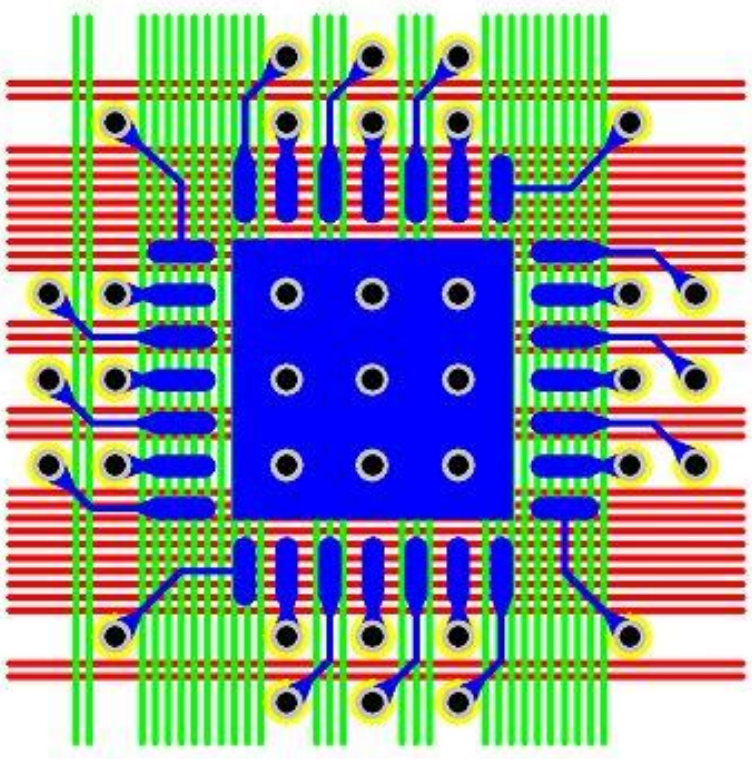


Figure 15. Sample fanout for 0.65mm QFN.

Figure 16 is a 0.5 mm QFN via fanout and routing channel solution. This routing solution provides for 2 traces between vias.

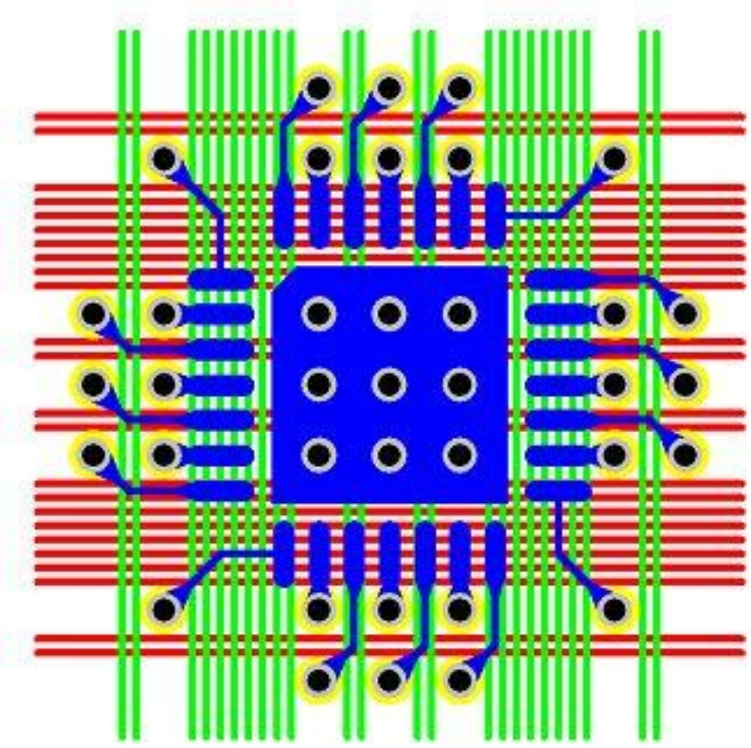


Figure 16. Sample fanout for 0.5mm QFN.

Figure 17 is a 0.4 mm QFN via fanout and routing channel solution. This routing solution provides for 1 trace between vias.

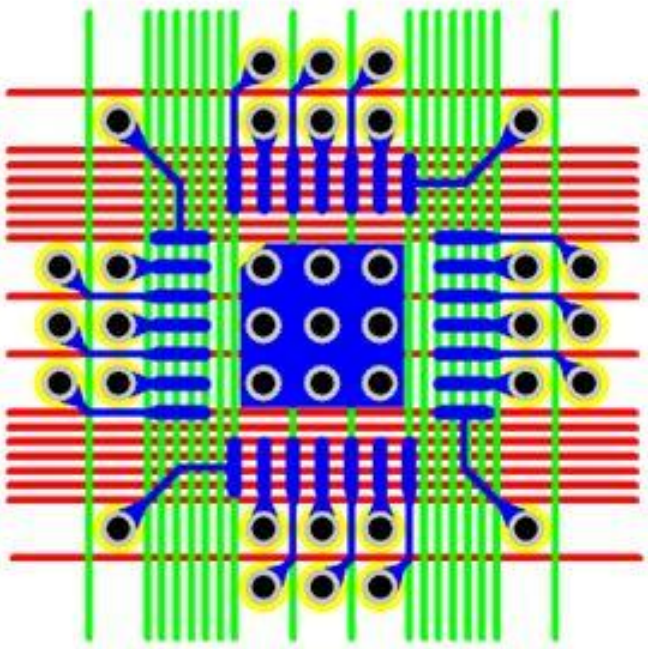


Figure 17. Sample fan out for 0.4mm QFN.

Download the 10-day evaluation license for **LP Wizard** and see how many different QFN library parts you can build.

Imperial or Metric PCB Design Units?

For my next two columns, I'm going to diverge a bit from my normal format to give you a little variety in your reading material. Instead of talking about components, land patterns and the like, this column and the next will address a topic that is one of my passions: The metric system.

If the French had won the French and Indian War (1756-1763, also known as the Seven Years War) against the British, imperial units or the English measurement system would not exist in society today. Yet even the British transitioned to the metric measurement system 46 years ago. America is the last stronghold for the imperial measurement system.

How much longer will it take for the world to become united under a single measurement system? That's what it's going to take to fully automate all of our PCB processes – a global measurement system.

The metric unit system is one of the greatest secrets to PCB design perfection today. From 1974-1991, we used inch units for our PCB layout. From 1991-2001, we used mil units. From 2001-2011 we used millimeter units. I have to say that when we made the transition from mils to millimeters, our productivity levels slipped a bit during the learning curve. But after five or six PCB layouts, our productivity was back to normal.

And after about 15 PCB layouts our productivity levels surpassed all previous results. If I were forced to go back to the mil measurement system, my productivity levels would reverse. There is no way in the world that anyone in 2011 using mil units can outperform the same talent using millimeter units, because most component pin pitches are on a millimeter grid system (like the 1 mm pitch BGA) and metric units are vastly superior to work within the PCB design space. All of the numbers are evenly divisible by 10 and there is no need for calculators for mathematical calculations.

No designer I know of who has successfully transitioned to the metric unit system for PCB layout wants to go back to the imperial unit system. That statement alone says it all.

Why is the US Still "Inching" Along?

I hear it all the time from corporations who will not convert: "We're American and we have our own measurement system. We are not part of the European Union or Russia or Japan. We're proud to be Americans and we believe in our way of life and the system and values that we use."

Well, let me shine a little light for proud Americans who do not know the historical facts. Most Americans believe that our involvement with metric measurement is relatively new. In fact, the United States has been increasing its use of metric units for many years, and the pace has accelerated in the past four decades.

In the early 1800s, under the presidency of Thomas Jefferson, the US Coast and Geodetic Survey (the government's surveying and map-making agency, now known simply as the **National Geodetic Survey**) used meter and kilogram standards brought from France. Abraham Lincoln was a strong proponent of the metric unit system and in 1866, one year after Lincoln's assassination, Congress authorized the use of the metric system in America and supplied every state with a set of standard metric weights and measures.

In 1875, the United States solidified its commitment to the development of the internationally recognized metric system by becoming one of the original 17 signatory nations to the **Treaty of the Metre** (Convention du Mètre). As a matter of fact, there would not be imperial units in the world today if the US Congress had fulfilled the commitment that the country agreed to at that convention.

The signing of this international agreement concluded five years of meetings in which the metric system was reformulated, refining the accuracy of its standards. The Treaty of the Metre established the **International Bureau of Weights and Measures** (BIPM) in Sèvres, France, to provide standards of measurement for worldwide use.

In 1893, metric standards – developed through international cooperation under the auspices of BIPM – were adopted as the fundamental standards for length and mass in the United States. Our customary measurements – the foot, pound, quart, etc. – have been defined in relation to the meter and the kilogram ever since. The General Conference of Weights and Measures, the governing body that has overall responsibility for the metric system, and which is made up of the Treaty of the Metre signatory nations, approved an updated version of the metric system in 1960. This modern system is called Le Système International d'Unités or the International System of Units, abbreviated SI.

The United Kingdom began a transition to the metric system in 1965 to more fully mesh its business and trade practices with those of the European Common Market. The conversion of the United Kingdom and the Commonwealth nations to SI created a new sense of urgency regarding the use of metric units in the United States.

The US Begins Transition

In 1968, Congress authorized a three-year study of systems of measurement in the U.S., with particular emphasis on the feasibility of adopting SI. The detailed US Metric Study was conducted by the Department of Commerce. A 45-member advisory panel consulted with and took testimony from hundreds of consumers, business organizations, labor groups, manufacturers, and state and local officials.

The final report of the study, **A Metric America: A Decision Whose Time Has Come** concluded that the US would eventually join the rest of the world in the use of the metric system of measurement. The study found that measurement in the United States was already based on metric units in many areas and that it was becoming more so every day. The majority of study participants believed that conversion to the metric system was in the best interests of the nation, particularly in view of the importance of foreign trade and the increasing influence of technology in American life.

The study recommended that the US implement a carefully planned transition to predominant use of the metric system over a ten-year period. Note: In 1975, the Australian continent also implemented its metric conversion act and successfully transitioned. The United States Congress passed the **Metric Conversion Act of 1975** "to coordinate and plan the increasing use of the metric system in the United States." The Act, however, did not require a 10-year conversion period.

A process of voluntary conversion was initiated, and the US Metric Board was established. The Board was charged with "devising and carrying out a broad program of planning, coordination, and public education, consistent with other national policy and interests, with the aim of implementing the policy set forth in this Act."

The efforts of the Metric Board were largely ignored by the American public, and, in 1981, the Board reported to Congress that it lacked the clear Congressional mandate necessary to bring about national conversion. Due to this apparent ineffectiveness, and in an effort to reduce federal spending, the Metric Board was disbanded in the fall of 1982.

The Board's demise increased doubts about the United States' commitment to metrication. Public and private sector metric transition slowed at the same time that the very reasons for the United States to adopt the metric system – the increasing competitiveness of other nations and the demands of global marketplaces – made completing the conversion even more important.

A New Attempt

Congress, recognizing the necessity of the United States' conformance with international standards for trade, included new encouragement for U.S. industrial metrication in the Omnibus Trade and Competitiveness Act of 1988. This legislation amended the Metric Conversion Act of 1975 and designates the metric system as “the preferred system of weights and measures for United States trade and commerce." The legislation states that the Federal Government has a responsibility to assist industry, especially small business, as it voluntarily converts to the metric system of measurement.

Federal agencies were required by this legislation, with certain exceptions, to use the metric system in their procurement, grants and other business-related activities by the end of 1992. While not mandating metric use in the private sector, the federal government has sought to serve as a catalyst in the metric conversion of the country's trade, industry, and commerce.

The current effort toward national metrication is based on the conclusion that industrial and commercial productivity, mathematics and science education, and the competitiveness of American products and services in world markets will be enhanced by changing to the metric system. Failure to complete the change will increasingly handicap the nation's industry and economy.

I would like to clarify to the reader that I’m not proposing that we change the American way of life, or change measurements in our sports (football, baseball, golf, etc.) or the cooking units used in our kitchens.

But the electronics industry must change in order to increase our competitiveness with the rest of the world. And, America has an impact on other counties’ weights and measurement systems. The EU Metric Directive (80/181/EEC), scheduled to go into effect on January 1, 2010, has been modified to allow the continuation of both supplemental (US customary, inch-pound) and metric units for consumer goods sold in the EU. The rule was published on May 7, 2009 in the Official Journal of the European Union.

The modified Directive instructs the European Commission to produce a report to the Parliament and Council regarding the smooth functioning of the internal market and international acceptance of SI units by December 31, 2019, including proposals where appropriate. Demonstrated progress will be important for achieve long-term acceptance of supplemental units in the EU. Modifying the US Fair Package and Labeling Act (FPLA) to permit metric labeling is an example where greater international marketplace acceptance of SI units can be achieved.

In Part B of this column, I will present imperial-to-metric conversion charts as they apply to PCB design. I will also post a short message on the proper terminology that I refer to as Metric Etiquette.

Inch-to-Metric Conversion Tables

First, let me start out with a few tips about metric speak that all PCB designers need to know. Metric is not a unit of measure. Metric is a term that describes a measurement system. You use either millimeters or micrometers for your PCB design units. The proper terminology to describe your working units when using the metric measurement system is millimeters or micrometers, not metric. For example: When doing PCB layout in inches or mils, you never refer to working in "imperial units." The same holds true with metric.

Millimeters allow finer (and greater) granularity in the PCB design grid system to optimize board real-estate, part placement, via fanout and routing trace/space features and snap grids. This will be very important in the future of PCB RF microtechnology. PCB impedance measurements are more accurate in micrometer units than "ounces of copper" and mil core/prepreg dielectric. Use micrometer units to achieve the highest level of accuracy for impedance calculations.

Why Hasn't Metric Caught On?

Unfortunately, PCB manufacturers are directly responsible for holding back the progress in the transition to metrication of our industry. When the PCB fabrication companies transition to the metric system, the entire electronics industry will achieve the peak of electronic product development automation. Until then, we'll plod along using dual units in the land of chaos.

Chip Component Names	
Millimeter	Inch
0402	01005
0603	0201
1005	0402
1608	0603
2013	0805
3216	1206
5025	2010

Table 1

Here is an example of the chaos in the chip component family. All chip names refer to their body length and width. When EIAJ introduced the standard chip and molded body component dimensions, only millimeter units were used. A 3216 was 3.2 mm long and 1.6 mm wide. It was all very simple. When the data was passed on to EIA in America, they changed all the chip names from millimeters to Inches and a 3216 was renamed 1206 or 0.125" length and 0.062" width (just drop the third-place number). Today most component manufacturers dimension all of their component packages in millimeters (see Table 1 for illustration of metric vs. imperial names.) You can easily see the confusion in the dual measurement system.

How to Move Forward

Let's start the transition process. Fully 99% of all PCB layouts use vias. See Table 2 for an inch to millimeter conversion chart for common via sizes, starting with a 0.15 mm hole and growing in 0.05 mm increments. I'll provide the entire padstack conversion. I intentionally did not add thermal relief data because vias should have a direct plane connection (no thermal relief is necessary). When transitioning from imperial units to metric units, always round off the millimeter values in 0.05 mm increments for normal resolution. If you're working on extremely dense handheld device technology, round off to the

nearest 0.01 mm. For PCB design, there is no reason to go more than two places to the right of the decimal point for the present. Remember, 0.01 mm = 0.0003937”.

VIA PADSTACK TECHNOLOGY							
HOLE SIZE		PAD SIZE		PLANE CLEARANCE		SOLDER MASK	
INCH	METRIC	INCH	METRIC	INCH	METRIC	INCH	METRIC
0.006”	0.15 mm	0.016”	0.40 mm	0.024”	0.60 mm	0.000”	0.00 mm
0.008”	0.20 mm	0.018”	0.45 mm	0.026”	0.65 mm	0.000”	0.00 mm
0.010”	0.25 mm	0.020”	0.50 mm	0.028”	0.70 mm	0.000”	0.00 mm
0.012”	0.30 mm	0.024”	0.65 mm	0.030”	0.75 mm	0.000”	0.00 mm
0.014”	0.35 mm	0.028”	0.70 mm	0.032”	0.80 mm	0.000”	0.00 mm
0.016”	0.40 mm	0.030”	0.75 mm	0.034”	0.85 mm	0.016”	0.40 mm
0.018”	0.45 mm	0.033”	0.85 mm	0.036”	0.90 mm	0.018”	0.45 mm
0.020”	0.50 mm	0.035”	0.90 mm	0.038”	0.95 mm	0.020”	0.50 mm
0.022”	0.55 mm	0.040”	1.00 mm	0.040”	1.00 mm	0.022”	0.55 mm
0.024”	0.60 mm	0.043”	1.10 mm	0.042”	1.05 mm	0.024”	0.60 mm

Table 2

Table 3 illustrates four common inch-based part placement grids and their millimeter equivalents. The common rule in placing parts in millimeters is to always stay one place to the right of the decimal or 0.1 mm increments.

COMPONENT PLACEMENT		
SNAP GRIDS		PART PLACEMENT
INCH	METRIC	USES & SIZES
0.005”	0.10 mm	Very Dense Parts
0.025”	0.50 mm	Discrete Parts
0.050”	1.00 mm	IC’s & Large Parts
0.100”	2.00 mm	Very Large Parts

Table 3

Table 4 provides all the common trace/space technology and routing snap grids. The common rule when working in millimeters is to always use a 0.05 mm routing grid. Most component lead pin pitches are 0.05 mm increments and IPC-7351B land (pad) sizes and snap grids are in 0.05 mm increments. This totally optimizes trace routing and eliminates wasted PCB real estate. Everything fits together tighter than Lego building blocks.

Notice that in the inch units, a gridless shape-based option is used, but in millimeters all objects can easily snap to a grid and still achieve maximum density solutions. I provide three various route snap grid solutions for the various trace/space rules.

Note: Inch-based routing grids are evenly divisible into 0.100” while millimeter based routing grids are evenly divisible into 1 mm.

TRACE WIDTHS & OPTIMUM ROUTING GRIDS							
TRACE WIDTHS		ROUTE GRID #1		ROUTE GRID #2		ROUTE GRID #3	
INCH	METRIC	INCH	METRIC	INCH	METRIC	INCH	METRIC
0.004"	0.10 mm	0.001"	0.05 mm	0.000"	0.10 mm	0.000"	0.01 mm
0.005"	0.125 mm	0.005"	0.05 mm	0.001"	0.125 mm	0.000"	0.01 mm
0.006"	0.15 mm	0.00625"	0.05 mm	0.001"	0.01 mm	0.000"	0.00 mm
0.008"	0.20 mm	0.00833"	0.05 mm	0.005"	0.10 mm	0.001"	0.01 mm
0.010"	0.25 mm	0.005"	0.05 mm	0.001"	0.01 mm	0.000"	0.00 mm
0.012"	0.30 mm	0.0125"	0.05 mm	0.00625"	0.10 mm	0.001"	0.01 mm
0.015"	0.40 mm	0.005"	0.05 mm	0.001"	0.10 mm	0.000"	0.01 mm
0.020"	0.50 mm	0.005"	0.05 mm	0.001"	0.10 mm	0.000"	0.01 mm
0.030"	0.75 mm	0.005"	0.05 mm	0.001"	0.10 mm	0.000"	0.01 mm
0.040"	1.00 mm	0.005"	0.05 mm	0.001"	0.25 mm	0.000"	0.10 mm

Table 4

Table 5 provides the PCB material equivalents. Note that the various columns are not related to each other. Each column describes a specific PCB feature. In the first column "board thickness" is common PCB finished material thickness, and the metric equivalents are rounded off to the nearest 0.1 mm. The second column is copper weight in ounces and their micrometer equivalent. Using micrometers to describe copper thickness is better than using weight. The third and forth columns go together. Column 3 defines the type of hole and column 4 provides the PCB fabrication tolerance for each different hole type in the chart.

PC BOARD CRITERIA							
BOARD THICKNESS		COPPER THICKNESS			HOLE TYPE DESCRIPTION	HOLE SIZE TOLERANCES	
INCH	METRIC	OUNCE	INCH	METRIC		INCH	METRIC
0.020"	0.50 mm	¼ OZ.	0.00035"	9um	Via < 0.35mm	+0 –Hole Size	+0 –Hole Size
0.031"	0.80 mm	½ OZ.	0.0007"	18um	Via > 0.35mm	±0.003"	±0.08 mm
0.040"	1.00 mm	1 OZ.	0.0014"	35um	Plated Hole	±0.003"	±0.08 mm
0.062"	1.60 mm	1 ½ OZ.	0.0021"	53um	Non-plated Hole	±0.002"	±0.05 mm
0.070"	1.80 mm	2 OZ.	0.0028"	70um	Slotted Hole	±0.005"	±0.13 mm
0.093"	2.30 mm	3 OZ.	0.0042"	105um	NPT Tooling Hole	±0.001"	±0.03 mm

Table 5

Table 6 is common plated through-hole padstacks for component leads and their inch-to-millimeter conversion. All hole, pad and plane clearance values are in 0.05mm increments. The solder mask is the same value as the outer layer pads. This padstack information was taken from the proportional padstack table and you can download it **here** under "Appnote 10836: Proportional Through-hole Padstacks."

Note: this downloadable chart only contains millimeter values and not the inch equivalents in Table 6.

COMMON PLATED THROUGH COMPONENT PADSTACKS							
HOLE SIZE		PAD SIZE		PLANE ANTI-PAD		SOLDER MASK	
INCH	METRIC	INCH	METRIC	INCH	METRIC	INCH	METRIC
0.020"	0.50 mm	0.040"	1.00 mm	0.050"	1.25 mm	0.040"	1.00 mm
0.028"	0.70 mm	0.050"	1.20 mm	0.060"	1.50 mm	0.050"	1.20 mm
0.035"	0.90 mm	0.055"	1.40 mm	0.065"	1.70 mm	0.055"	1.40 mm
0.040"	1.00 mm	0.060"	1.50 mm	0.070"	1.80 mm	0.060"	1.50 mm
0.047"	1.20 mm	0.070"	1.80 mm	0.080"	2.05 mm	0.070"	1.80 mm
0.052"	1.30 mm	0.080"	2.00 mm	0.085"	2.15 mm	0.080"	2.00 mm
0.057"	1.40 mm	0.085"	2.10 mm	0.090"	2.25 mm	0.085"	2.10 mm
0.062"	1.60 mm	0.095"	2.40 mm	0.095"	2.50 mm	0.095"	2.40 mm

Table 6

Table 7 is common non-plated through-hole padstacks and their inch-to-millimeter conversion. All hole, pad and plane clearance values are in 0.05 mm increments. The solder mask is the same value as the hole size to allow the PCB manufacturer to oversize it per their specific fabrication tolerances. Notice that the pad size for every padstack is 1.00 mm. Because the holes are not plated, the hole size is typically larger than the hole size. Also, there is no reason to have multiple pad sizes when the pad is eventually drilled away. The only reason for having a pad in a non-plated padstack is to display a marker as a guide for the hole location. The PCB manufacturer does not need the pad in the padstack, but sometimes when there is no pad (but there is a drill hole) the manufacturer might question whether the hole is valid. Of course, there is no thermal relief required in non-plated hole padstacks.

COMMON NON-PLATED PADSTACKS							
HOLE SIZE		PAD SIZE		PLANE ANTI-PAD		SOLDER MASK	
INCH	METRIC	INCH	METRIC	INCH	METRIC	INCH	METRIC
0.062"	1.60 mm	0.040"	1.00 mm	0.105"	2.50 mm	0.062"	1.60 mm
0.093"	2.40 mm	0.040"	1.00 mm	0.135"	3.35 mm	0.093"	2.40 mm
0.098"	2.50 mm	0.040"	1.00 mm	0.140"	3.45 mm	0.098"	2.50 mm
0.110"	2.80 mm	0.040"	1.00 mm	0.155"	3.80 mm	0.110"	2.80 mm
0.125"	3.20 mm	0.040"	1.00 mm	0.170"	4.25 mm	0.125"	3.20 mm
0.156"	4.00 mm	0.040"	1.00 mm	0.200"	5.10 mm	0.156"	4.00 mm
0.187"	4.80 mm	0.040"	1.00 mm	0.230"	6.00 mm	0.187"	4.80 mm

Table 7

I want to note that the LP Calculator (available **here** **)** automatically performs all of these padstack calculations for you and provides 5 different options:

1. Proportional Environment
2. IPC-7251 Most Environment
3. IPC-7251 Nominal Environment

4. IPC-7251 Least Environment
5. User Defined Environment Rules

Reference Designators

Drafting elements in a CAD library part are not “standardized” for specific values or sizes. But recommendations coming out in the IPC-2610 series include schematics, PCB assembly and fabrication. Documentation includes component outline and polarity markings for silkscreen and assembly. This article focuses on silkscreen and assembly reference designators.

Every reference designator (ref des) originates in the schematic diagram and is transferred to the PCB layout via the netlist. They also appear in the Bill of Materials that is exported from the schematic and passed to the assembly shop. The rules for reference designator assignment are established by IPC-2512. However, the ref des size, font, CAD layer and placement location are left up to the EE engineer and/or PCB designer.

Reference Designators in the CAD Library

Every CAD library part should possess two distinct reference designators: One for the silkscreen and one for the assembly drawing. Both designators, in every CAD library part, are normally located in the center of the component body. The silkscreen reference designator is relocated outside the component body after the part placement is completed and approved by the design review panel. If via fanout and trace routing cause part placement nudging, then it’s best to wait until that process is completed or duplication of effort will come into play.

Also, if via hole sizes exceed 0.4 mm and they are not tented, then it’s best to avoid placing the silkscreen reference designators over the via hole; the ink will drop into the hole, making the reference designator indistinguishable and eliminating the purpose for the reference designator to begin with. If you are using large via hole sizes, it’s best to wait until the PCB design passes the engineering routing review panel. Via sizes smaller than 0.4mm can be tented (covered) with solder mask and the placement of silkscreen designators can go directly on the via.

The silkscreen reference designator height sizes are:

- 1.0 mm - Minimum
- 1.5 mm - Default
- 2.0 mm - Nominal
- 2.5 mm - Maximum

The reference designator text line width is normally 10% of the height for good clarity and to prevent the characters from bleeding or blobbing together. The 0.15 mm height “default” is what the LP Calculator uses, but users can change the global setting values to any value or measurement system.

The assembly reference designators are different, in that they are never relocated outside the component body outline. Assembly reference designator height sizes are:

- 1.5 mm – Default
- 1.2 mm – 0.5 mm for miniature components

Here are some chip component assembly ref des height sizes that scale down according to the body size:

- 4520 (EIA 1808) = 1.5 mm
- 3216 (EIA 1206) = 1.2 mm
- 2013 (EIA 0805) = 1.0 mm

- 1608 (EIA 0603) = 0.7 mm
- 1005 (EIA 0402) = 0.5 mm
- 0603 (EIA 0201) = 0.5 mm

Note: All assembly body outlines are 1:1 scale of the physical component with the exception of all micro-miniature parts smaller than 1.6 mm length. Parts less than 1.6 mm length are EIA 0402 and 0201; their assembly outlines have to be enlarged so that the 0.5 mm assembly ref des fits cleanly inside them.

Also, most land patterns (CAD library parts) have the lands (pads) on the assembly layer. This is true for all parts that are large enough to accommodate both the component leads and the assembly ref des without interfering with each other. When the component leads interfere with the assembly ref des, the component leads on the assembly layer are removed from the padstack. This includes all chip components, crystals, molded body parts and grid array parts with bottom only leads.

See Figure 1 for a sample of a typical silkscreen with the reference designators relocated outside the part.

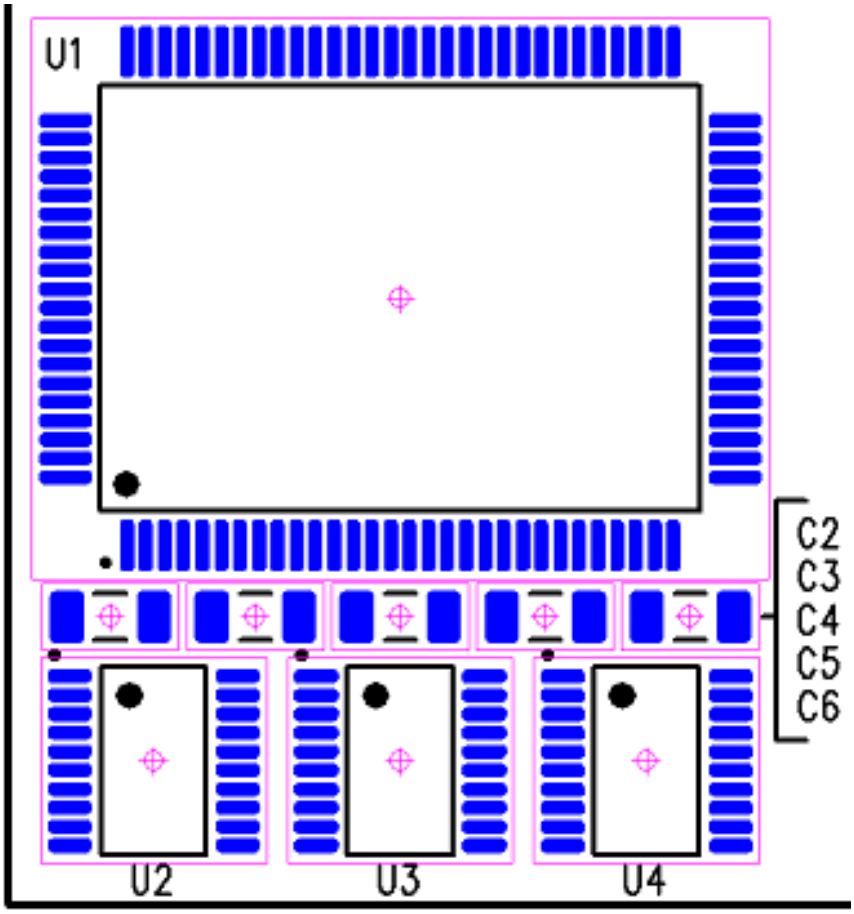


Figure 1. Typical silkscreen with reference designators outside the part placement.

See Figure 2 for a sample of a typical assembly drawing with the reference designators inside the part, exactly where they were put when the CAD library parts were built.

While the silkscreen reference designators must be relocated to an optimized location after part placement, the assembly reference designators do not require any movement or cleanup.

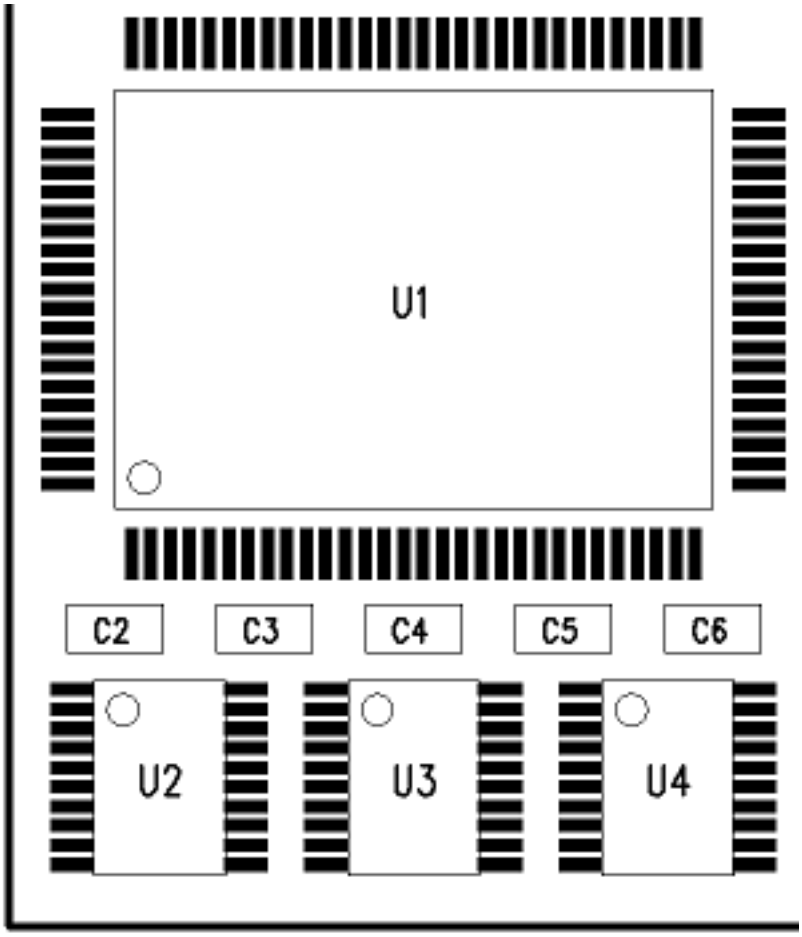


Figure 2. Typical assembly drawing with the reference designators inside the part.

Also, notice in Figure 2 that the large parts have lands (pads) built into the padstack and the small chip components do not have lands on the assembly layer. The LP Calculator allows the user to turn “Land” on and off, because some people do not want any component leads on the assembly drawing; they only want closed polygons with reference designators inside.

Table 1 contains list of the standard reference designators from the IPC-2612 standard for schematic symbol generation.

A	separable assembly
AR	amplifier
AT	attenuator; isolator
B	blower, motor
BT	battery
C	capacitor
CB	circuit breaker
CP	connector adapter, coupling
CN	capacitor network
D or CR	diode
D or VR	breakdown diode
DC	directional coupler
DL	delay line
DS	display, lamp
E	terminal
F	fuse
FD*	fiducial
FL	filter
G	generator, oscillator
GN	general network
H	hardware
HY	circulator, directional coupler
J	connector, jack, female
K	contactor, relay
L	coil, inductor, bead, ferrite bead
LS	loudspeaker, buzzer
M	meter
MG	motor-generator
MH*	mounting hole
MK	microphone
MP	mechanical part
P	connector, plug, male
PS	power supply
Q	transistor
R	resistor
RN	resistor network
RT	thermistor
S	switch
T	transformer
TB	terminal board, terminal strip
TC	thermocouple
TP**	test point, In-circuit test points
TZ	transzorb
U	inseparable assembly, IC pkg
V	electron tube
VR	voltage regulator
W	wire, cable, cable assembly
X	fuse holder, lamp holder, socket
Y	crystal, magnetostriction oscillator
Z	miscellaneous

Table 1.

**These class letters would not appear in a parts list as they are part of a PCB and not an active electronic component.*

***Not a class letter, but commonly used to designate test points for maintenance purposes.*

Note: The above list is not exhaustive. See the standard list of class designation letters in ANSI Y32.2/IEEE Std 315, Section 22 and the Index.

Padstack Naming Convention, Part 1

IPC introduced a new padstack naming convention in the IPC-7351B standard publication, and it is used exclusively in the Mentor Graphics LP calculator. This is the first of three columns that explain the breakdown of the new standard and its benefits.

The padstack consists of combinations of letters and numbers that represent shape or dimensions of lands on different layers of printed boards or documentation. The name of the padstack must represent all the various combinations. These are used in combination with the land pattern conventions defined herein according to the rules established in the IPC-2220 design standards.

The first part of the padstack convention consists of a land (pad) shape. There are six basic land shape identifiers. *Note*: All alphabetical characters are lower case. This helps discriminate numeric values.

The basic land shape identifier letters:

c = Circular
s = Square
r = Rectangle
b = Oblong
d = D-shape (square on one end and circular on the other end)
u = User-defined contour (irregular shape)

The "**b**" was used for oblong because the letter "**o**" can easily be confused with the character zero "**0**".

The next section of the naming convention addresses assumed defaults. This is to keep the default padstack name short and simple. Any deviations from these padstack defaults require the use of special modifiers.

- Solder mask is 1:1 scale of the land size
- Paste mask is 1:1 scale of the land size
- The assembly layer land is 1:1 scale of the land size
- Inner layer land is the same shape as the outer layer land
- The primary and secondary lands are the same size
- The inner layer land shapes are circular
- Vias are circular
- Thermal ID, OD and spoke width sizes follow the IPC Level A, B or C
- Thermal reliefs have 4 spokes
- Plane clearance anti-pad size follows the IPC Level A, B or C
- Mounting holes are circular

Every board fabricator's ability to register solder mask is different. The 1:1 scale solder mask default compensates for this variation, as long as manufacturers are building to standard specifications such as the IPC-6012 which states that you can't have misregistration of the solder mask.
When you are creating a CAD library that will be used for various trace/space combinations, it's important that you leave the responsibility of the solder mask swell up to the CAM operators when they are panelizing your ODB++ or Gerber data. By having all of the solder mask sizes set to 1:1 scale of the land (pad) size, you are providing the manufacturer with a known starting point to work with.

Padstack Naming Convention, Part 2

Last week, I introduced padstack naming conventions. This week I'll delve more specifically into these conventions. As with most things, there are exceptions to the rules, so let's start with an exception to last week's rules.

There is an exception to the rule for creating solder mask-defined lands for BGAs. IPC does not recommend solder mask-defined BGA CAD library parts but some companies use this technique for very-fine-pitch parts that require a small diameter land size.

In this case, the solder mask acts as an adhesive to secure the land to the prepreg to help withstand drop testing for handheld electronic products. It has been proven in drop tests for handheld electronic devices that a fine-pitch BGA solder joint is more secure than the land attachment to the prepreg. During drop testing, a fine-pitch BGA pad will rip away from the PCB prepreg material before the BGA solder joint fails. See Figure 1 for an example of a solder mask-defined BGA land.

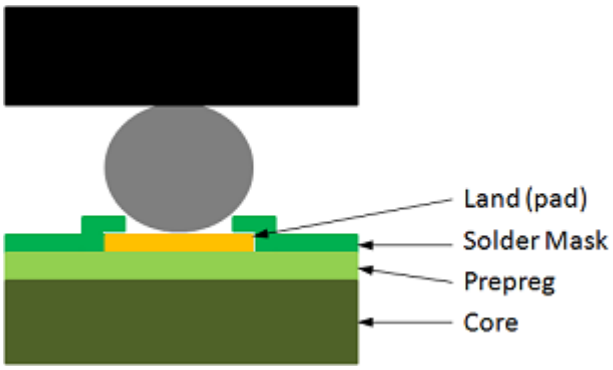


Figure 1. A solder mask-defined BGA land.

Solder mask-defined lands are also used for flexible circuit boards for the same reason – to hold the land (pad) to the PCB surface to prevent the land from ripping away from the PCB material. When you use solder mask-defined lands you must indicate which parts deviate from the 1:1 scale solder mask rule in the fabrication drawing notes. This notifies the CAM operator not to swell these solder mask features.

In the padstack naming convention, there are illegal characters that should never be used. These include " " , ; : / \ [ ] ( ) . { } * & % # $! @ ^ =

Examples utilizing the "Basic Land Shape Letters" (**all padstack values are in metric units**)

Note: Every number goes two places to the right and as many places as needed to the left of the decimal.

For example: 1150 = 11.50 mm or 11500 µm, 150 = 1.50 mm or 1500 µm, 15 = 0.15 mm or 150 µm

c150h90 - where "c" denotes a circular land with a 1.50 diameter and H denotes a hole size of 0.90

v50h25 - where a "v" denotes a via with a 0.50 land (default circular land) and H denotes a 0.25 hole

s150h90 - where "s" denotes a 1.50 square land and H denotes a hole size of 0.90

s350 - where 's" denotes a square SMT land size of 3.50

r200_100 - where “r” denotes a rectangular SMT land 2.00 land length X 1.00 land width

b300_150 - where “b” denotes a SMT oblong land size of 3.00 X 1.50

b400_200h100 - where “b” denotes an oblong land size of 4.00 length X 2.00 width and 1.00 hole

d300_150 - where “d” denotes land with one circular end and one square end (looks like a D) 3.00 X 1.50

v30h15l1-3 - where “v” denotes a 0.30 blind via with 0.15 Hole; 1 is the starting layer, 3 is the end layer

r200_100r5 - Rounded rectangular 2mm X 1mm X 0.05mm radius corners

r200_100c10 - Chamfered rectangular 2mm X 1mm X 0.1mm chamfered corners

v30h15l3-6 - where “v” denotes a 0.30 buried via with 0.15 hole; 3 is the starting layer, 6 is the end layer

Special modifiers are used when padstack features are different than the defaults. These are the “variants” or “modifiers” that go after the basic padstack naming convention.

These are used when the user needs to change the padstack default values either by a different dimension or a different shape. In instances where shapes are different this becomes a two-letter code with the modifier first, followed by the land shape letter.

These are single-letter modifiers:

n = Non-plated hole

z = Inner layer land dimension if different than the land on primary layer

x = Special modifier used alone or following other modifiers for lands on opposite side to primary layer land dimension

t = Thermal relief; if different than IPC standard padstack – tid_od_sw for 4 spoke default

m = Solder mask if different than default 1:1 scale of land

p = Solder paste if different than default 1:1 scale of land

a = Assembly surface land if different than default 1:1 scale of land

y = Plane clearance (anti-pad) if the value is different than the thermal OD

o = Offset land origin

k = Keep-out

r = Radius for rounded rectangular land shape

c = Chamfer for chamfered rectangular land shape

These are double-letter modifiers:

ts = Thermal square; if different than the top side land shape and dimensions

sw = Thermal spoke width

zs = Inner layer land shape is square (Note: The default is circular)

m0 = No solder mask

mxc = Solder mask opposite side circular

mx0 = Solder mask opposite side no solder mask

xc = Opposite side circular

vs = Via with square land

hn = Non-plated hole

Land shape change is the last letter in the string prior to the dimension.

Examples of single-letter modifiers with a circular plated through-hole land:

c150h90 = Default padstack with a 1.50 circular land with a 0.90 hole (no modifiers used)

c150hn90 = Default padstack with a 1.50 circular land with a 0.90 non-plated hole (no modifiers used)

c150h90z140 = Inner layer land is smaller than external lands 1.40 or 0.10 smaller

c150h90z140x170 = Opposite side land is larger than top side land 1.70 or 0.20 larger

c150h90z140x170m165mx185 = Solder mask opening for top and bottom lands 0.15 larger for each

c150h90z140x170m165mX185a200 = Assembly drawing land in 0.50 larger than 1.50 primary land

c150h90z140x170m165mx185a200y300 = Plane clearance anti-pad diameter is 3.00

c150h90z140x170m165mx85 = Solder mask encroachment on opposite land by 0.65 smaller

c150h90m165 = adding a solder mask opening of 1.65 diameter or 0.15 larger than land

c150h90t150_180_40 = Thermal ID 1.50, OD 1.80, spoke Width 0.40, Anti-pad 1.80

c150h90t150_180_40y200 = Anti-pad 2.00 (because the size is different than the Thermal OD)

c150h90t150_180_80_2 = Spoke width 0.80 with 2 spokes

c150h90m165t150_180_40 = Solder mask 1.65

c150h90zc150 = where “c” is circular 1.50 land with 0.90 hole with 1.50 inner (Z) layer circular land

Examples of single letter modifiers for surface mount land:

b300_150 = Default padstack with a 3.00 length and 1.50 width land (no modifiers used)

b300_150m330_180 = Solder mask is 0.30 larger than the land

b300_150m330_180p240_140 = Solder paste is smaller by 0.10 width and 0.60 length

b300_150b-50 = Oblong Land 3.0mm X 1.5mm w/offset origin negative 0.5mm

r400_200po430_230 = Rectangle SMT land 4.00 X 2.00 with an oblong solder paste size of 4.30 X 2.30

Examples of a padstack with oblong land with slotted hole:

Sample – **b** = Oblong land shape then “**X**” dimension (length) then Underscore _ “**Y**” dimension (width)

b400_200h300_100 = Oblong land 4mm length X 2mm width with slotted hole size 3mm X 1mm

b400_200hn300_100 = Oblong land 4mm X 2mm with non-plated slotted hole size 3mm X 1mm

Padstack Naming Convention, Part 3

Over the past two columns, we looked at padstack naming conventions, and some details. This week, I'll finish up the topic. Let's look at corner modifiers.

Chamfered and rounded corner modifiers are used to indicate which corners are modified. Figure 1 shows the "order of precedence" that has been given to the first four modifiers.

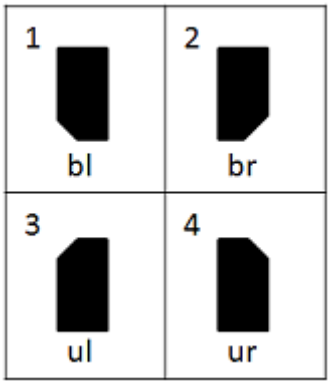


Figure 1.

Modifiers:

bl – bottom left
br – bottom right
ul – upper left
ur – upper right
ulr – upper left & right
blr – bottom left & right
ubl – upper and bottom left
ubr – upper and bottom right

Rounded and chamfered lands in "one corner" modifier examples:

r100_200rbl50 = rectangular land 1.00 x 2.00 with 0.50 radius for rounded corner in bottom left corner

r100_200rbr50 = rectangular land 1.00 x 2.00 with 0.50 radius for rounded corner in bottom right corner

r100_200rul50 = rectangular land 1.00 x 2.00 with 0.50 radius for rounded corner in upper left corner

r100_200rur50 = rectangular land 1.00 x 2.00 with 0.50 radius for rounded corner in upper right corner

r100_200cbl50 = rectangular land 1.00 x 2.00 with 0.50 chamfer for chamfer corner in bottom left corner

r100_200cbr50 = rectangular land 1.00 x 2.00 with 0.50 chamfer for chamfer corner in bottom right corner

r100_200cul50 = rectangular land 1.00 x 2.00 with 0.50 chamfer for chamfer corner in upper left corner

r100_200cur50 = rectangular land 1.00 x 2.00 with 0.50 chamfer for chamfer corner in upper right corner

The chamfered and rounded rectangular with all four corners chamfered does not need a corner modifier.

Modifier examples with rounded rectangle land shape:

r100_200r50 = rectangular land 1.00 x 2.00 with 0.50 radius for rounded corners in all 4 corners

r200_100r50 = rectangular land 2.00 x 1.00 with 0.50 radius for rounded corners in all 4 corners

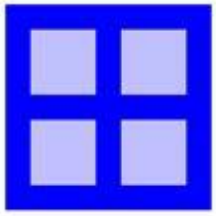
Modifier examples with chamfered rectangle land shape:

r200_100culr50 = rectangular land 2.00 x 1.00 with 0.50 chamfer for chamfered corners in 2 corners

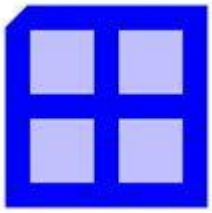
r200_100c50 = rectangular land 2.00 x 1.00 with 0.50 chamfer for chamfered corners in all 4 corners

Thermal pads can have a combination of chamfered and rounded corners; however, the typical application is two variations. The most prominent is a chamfered corner located near pin 1, and the second is a chamfered corner located near pin 1 with the other three corners rounded. These two variations are the default.

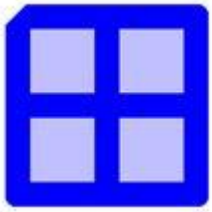
Square Configurations



s480p4s152 = 4.80mm square land with four paste mask squares measuring 1.52mm each



u480p4s152cul50 = 4.80mm square land with four paste mask squares of 1.52mm each with 0.50mm chamfer in upper left corner



u480p4s152cul50r25 = 4.80mm square land with four paste mask squares 1.52mm each with 0.50mm chamfer in upper left corner with 0.25mm corner radius

Example of a local fiducial for fine pitch SMT components:

c100m200k200 = Circular land 1.00 with solder mask 2.00 with keep-out 2.00

s100m200k200 = Square land 1.00 with solder mask 2.00 with keep-out 2.00

See Figure 2 for local fiducial application used for fine-pitch components.

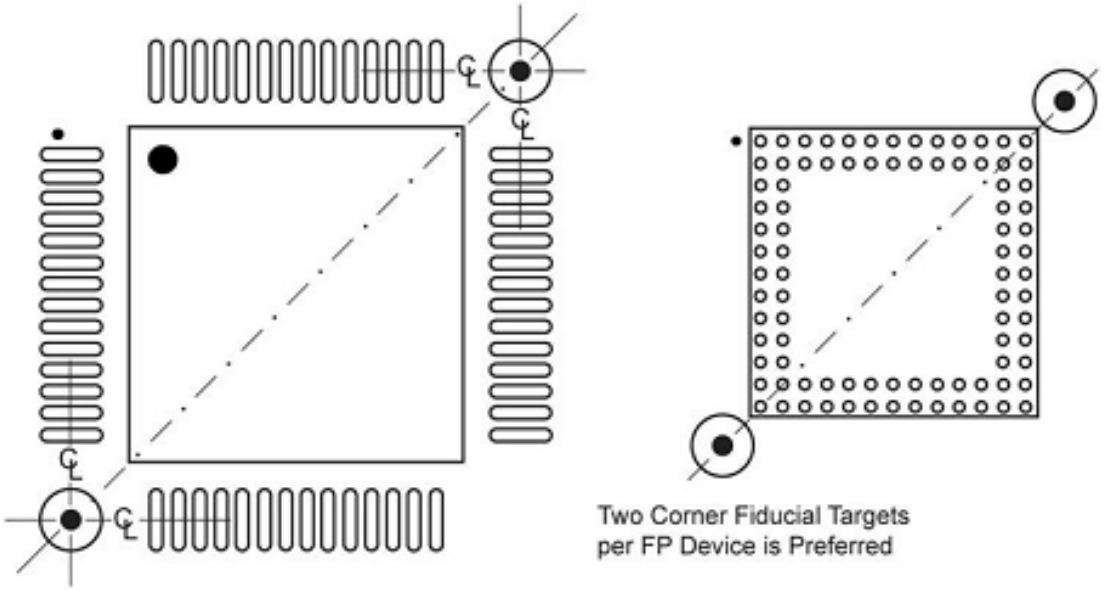


Figure 2.

Periphery Solder Joint Goals, Part 1

When it comes to solder joint goals, we are familiar with the terms toe, heel and side solder joint fillets, but IPC introduced the periphery solder joint in the latest release of the IPC-7351B.

Due to the introduction of several new component families like dual flat no-lead (DFN), land grid array (LGA), pull-back quad flat no-lead (PQFN), pull-back small outline no-lead (PSON) and column grid array (CGA), IPC created the periphery solder joint goal to accommodate these “bottom only terminal” lead forms as seen in Figure 1.

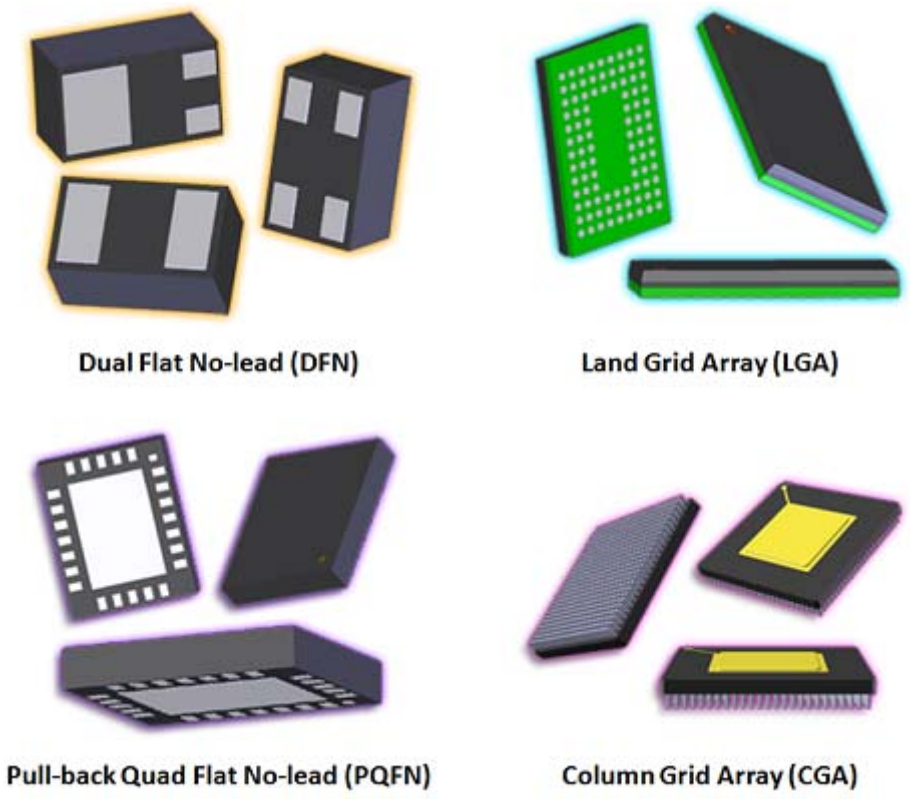


Figure 1.

The flat leads of these component families are very compatible with lead-free solder, due to the fact that some lead-free solder alloys have low-flow wetting properties. The flat lead with a periphery land area also improves assembly accuracy as the components have minimal “wander” movement during the reflow process. This is unlike the typical chip resistors and capacitors, which feature wraparound component leads.

Great caution must be taken into consideration because the J-STD-001D assembly standard allows for chip component overhang of up to 50% of the component width for Class 1 and Class 2 and 25% for Class 3 (the “A” dimension) as seen in Figure 2.

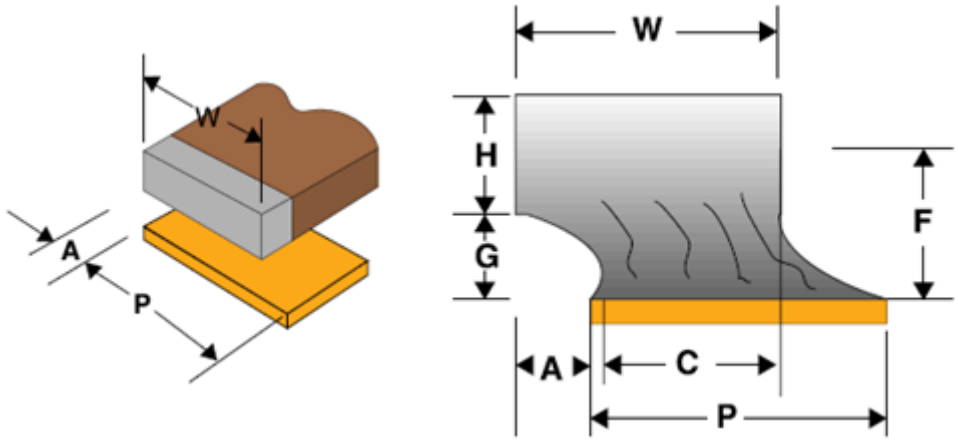


Figure 2.

The new DFN component family has 2-, 3- and 4-lead package styles and the body sizes range from 16 mm to 1 mm in size. The 2-pin DFN package is intended to replace wraparound leaded chip resistors, diodes and capacitors. The component terminal leads for pin 1 and 2 can be different sizes. The DFN component package data is derived from the JEDEC MO-236A standard. The 3-pin DFN package is intended to replace gull-wing leaded SOT23 and DPAK transistors and voltage regulators. The 4-pin DFN package is intended to replace a variety of different component families including oscillators, bridge rectifiers, LEDs, sensors, etc. The periphery solder joint goals as seen in Table 1 are used for the DFN, PSON and PQFN component families.

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Periphery	0.05	0.00	-0.05
Round-off Factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard Excess	0.5	0.25	0.1
Note: The rational for the "0.00 Nominal" and "-0.05 Least" environment is that the land size is compensated from the lead tolerance and fabrication and assembly tolerances.			

Table 1.

The LGA component family usage is rapidly growing. The LGA component lead style can be a bump, which is typically a round shape. But the LGA lead may also be flat, with a round, square or irregular shape. The pin assignments typically follow the same JEDEC convention as BGAs. The LGA component package data is derived from the JEDEC MO-270B standard. See Figure 3 for the LGA lead styles.

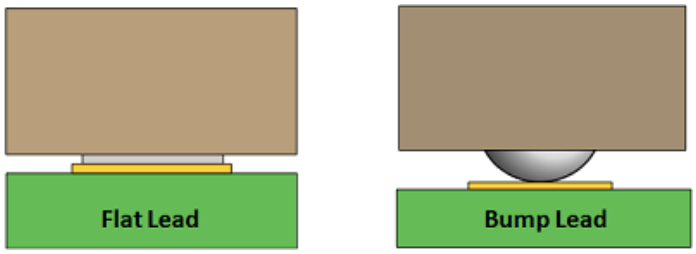


Figure 3.

See Figure 4 for the LGA lead shapes.

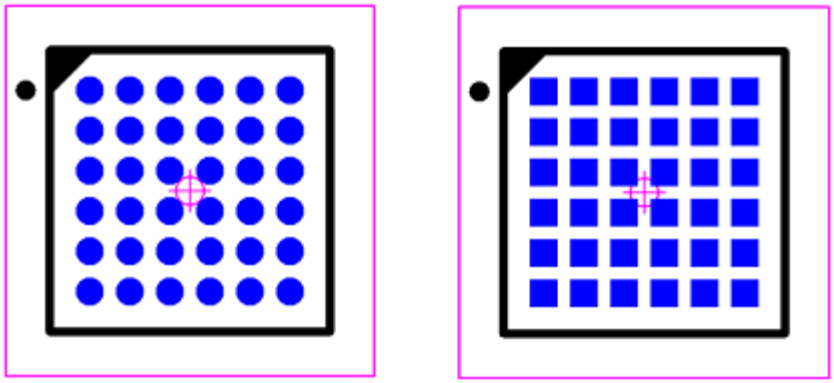


Figure 4.

The LGA land pattern only has one tier environment similar to the BGA however; the LGA land size is 1:1 scale of the lead size. See Table 2 for the LGA solder joint goals.

Lead Part	Median (Nominal) Density Level B
Periphery	0.00
Round-off Factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15
Courtyard Excess	1.00
Note: The rational for the "0.00 Periphery" is that the land size is compensated from the lead tolerance and fabrication and assembly tolerances.	

Table 2.

Multi-row and column LGAs will require via-in-pad routing solutions for the inner rows of contacts because there is no room for the traditional dog bone via fanout. Figure 5 represents a 1.0 mm pitch LGA with 0.7 X 0.7 mm square lands with a flat lead. You can place 0.5 mm pad & 0.25 mm hole vias in the center of the lands and be able to route two 0.1 mm traces between the vias.

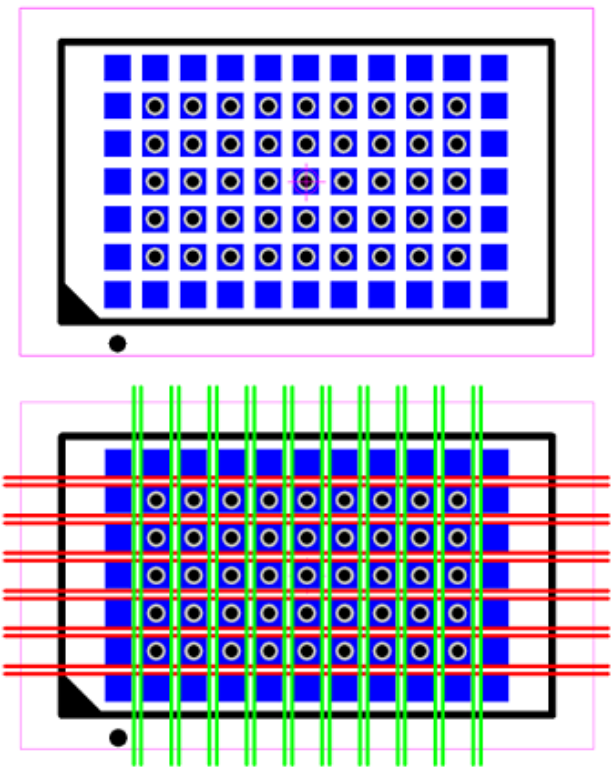


Figure 5.

Unlike pin grid arrays (PGA) that have been common to microprocessors, LGAs do not utilize any pins, but rather an array of bare gold-plated copper pads that permit a direct electrical connection between the component substrate and the PCB. Compared to the PGA component family, LGA pad density can be significantly higher due to tighter spacing that is not hindered by the need to attach pins to the substrate.

Linear Technology is the world's leading producer of LGA component packages. Linear uses unpopulated component leads in many of its component packages, as seen in Figure 6.

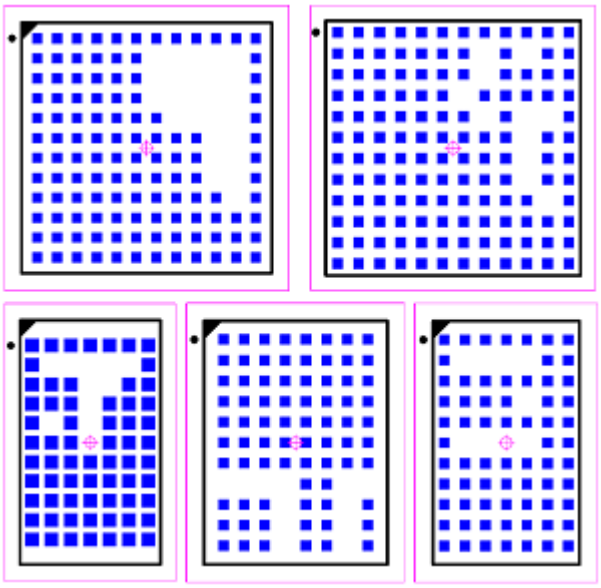


Figure 6.

Periphery Solder Joint Goals, Part 2

Let's move on to BGA packages. The BGA land is considered the first "periphery" land introduced to the electronics industry. However, the collapsing BGA ball is the only land calculation that creates a smaller land than the component lead. Non-collapsing BGA balls require a larger land size than the ball size.

Via-in-pad in a flat-lead LGA produces better solder joint results than BGA technology because there are no voids in the flat LGA component lead after reflow. Figure 1 is a BGA ball cross-section that illustrates trapped air holes using via-in-pad BGA void issues.

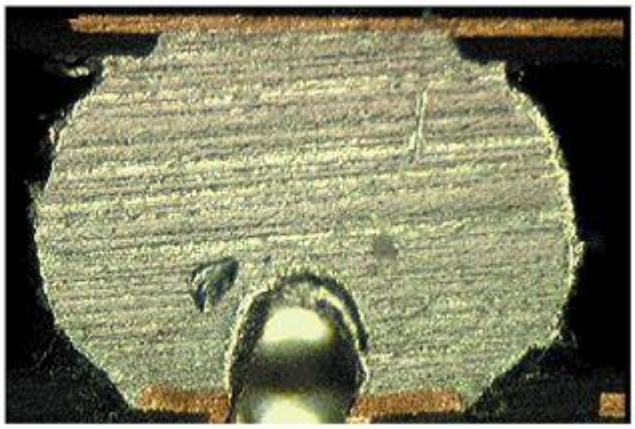


Figure 1. A BGA ball cross-section.

However, voids created by trapped air in blind or through-hole vias can be eliminated by plugging or filling the hole prior to the land plating process. Figure 2 illustrates various types of vias that contribute to trapped air and cause voids in BGA balls.

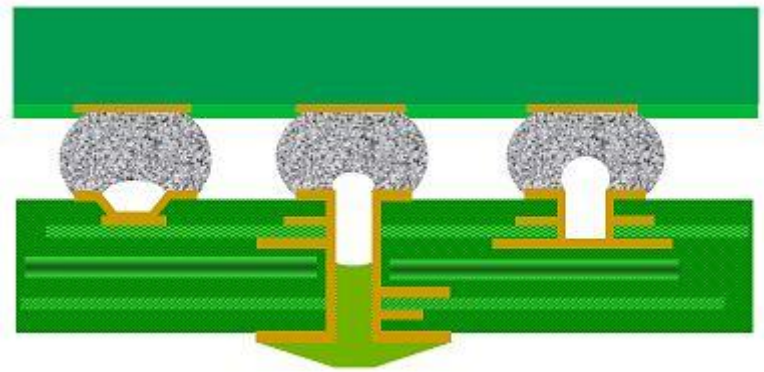


Figure 2. Types of vias that contribute to trapped air, causing voids.

The pull-back small outline no-lead package (PSON) is a rectangular semiconductor package with metal terminals along two sides of the bottom of the package. The pull-back leads are typically 0.1 mm to 0.2 mm away from the component body edge. The body of the component is generally molded plastic and the plastic mold compound is present on all 4 sides of the terminal lead contact. The SON and PSON component families are intended to replace the leaded SOIC, and they occupy about 50% less PCB area footprint. The PSON is considered a leadless package design with a bottom paddle to conduct heat away from the package using stitch vias that attach to the GND plane.

The pull-back component lead terminal shown in Figure 3 represents the PSON and the pull-back quad flat no-lead (PQFN) which have two different lead shapes, D-shape and rectangular. These illustrations are 0.8 mm pitch 5 mm X 5 mm body outline.

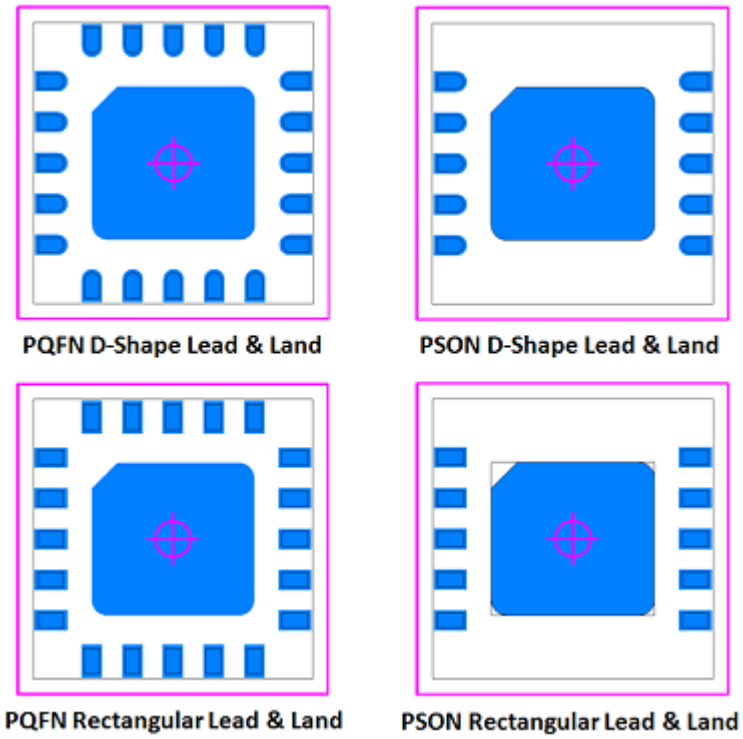


Figure 3. The pull-back component lead terminal.

Note: The latest LP Wizard and LP Calculator 10.3.1 release introduces the D-shape land calculation and CAD export to tools that support D-shape lands.

See Table 1 for the IPC-7351B 3-tier land pattern environments for PSON and PQFN component lead form with the periphery solder joint goals.

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Periphery	0.05	0.00	-0.05
Round-off Factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard Excess	0.5	0.25	0.1
Note: The rational for the "0.00 Nominal" and "-0.05 Least" environment is that the land size is compensated from the lead tolerance and fabrication and assembly tolerances.			

Table 1. The IPC-7351B 3-tier land pattern environments for PSON and PQFN component lead form.

Ceramic and plastic column grid arrays (CGA) solder column contacts are used for larger ceramic-based packages (32.0 mm to 45.0 mm). The package resembles the earlier plated through-hole pin-grid-array but with a closer contact pin pitch. The column contact diameter is typically 0.5 mm for 1.0 mm pin pitch and 1.2 mm to 2.0 mm lead length. The columns are attached to the package either by eutectic (Pb37Sn63) solder or they are cast in place using 90% Pb and 10% Sn. Via-in-pad technology is popular with the 1.0 mm pitch CGA component family due to the lack of room for a typical dog-bone via fanout.

The longer columns typically increase solder joint reliability by absorbing the stresses created by the CTE mismatch between the ceramic package and the PCB. On the other-hand, longer columns may reduce electrical performance and will increase the overall package profile on the PCB. Also, the columns are not as rugged as a BGA solder joint and are susceptible to handling damage.

The CGA was grouped with the LGA component family solder joint goals in the IPC-7351B at 1:1 scale lead-to-land size, but the CGA solder goals were recently been updated so that the land size is 0.1 mm larger than the maximum lead diameter.

Figure 4 illustrates the CGA solder joint goal with a periphery land to form a solder fillet and Table 2 features the solder joint goal data.

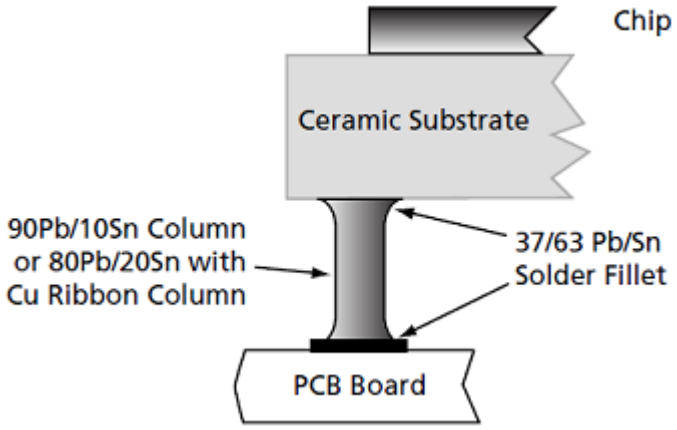


Figure 4. The CGA solder joint goal.

Lead Part	Median (Nominal) Density Level B
Periphery	0.10
Round-off Factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15
Courtyard Excess	1.00

Table 2. The solder joint goal data.

The DFN, PSON, PQFN, LGA, CGA and BGA present a different concept for developing land patterns. Effectively, there are no toe, side or heel fillets; instead, the land periphery is similar along the entire termination. Whether the component terminal shape is round, square, rectangle or D-shaped, once the tolerance is assigned it applies to the periphery of the lands for that particular part.

Thus the term “periphery” is used to signify that the principles occur all around the component package termination contact.